

Design and building of a 300 W MOSFET Push-Pull Power Amplifier for 144 MHz

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1. Introduction

Although valves are quite a common choice amongst the amateur community for building (high) power amplifiers, I opted for building a MOSFET Solid-State Power Amplifier (SSPA) instead. Indeed, for 144 MHz operation, I'm using a remote transverter located close to my antenna tower. So, in order to avoid setting-up a remote (subject to climatic variations) high voltage power supply, I preferred to build a low voltage powered solid-state amplifier. Here are the advantages and drawbacks of such an amplifier.

Advantages :

- No high voltage
- No heat-up time
- Less mechanical machining
- Lightweight equipment, easy to carry
- No retune needed (thermal drift)
- High MTBF

Drawbacks :

- Limited amount of power, unless paralleling amplifiers
- Expensive transistors
- The Gate is sensitive to electrostatic charges

The goal of this article is not only to describe such an amplifier but also to provide experimental guidelines to design a Push-Pull MOSFET amplifier.

The one described here is narrowband and provides more than 250 W RF power, for a current consumption of 18-20 A under 28 V.

2. Selection of the transistor

One could have selected two independent devices (of the same type of course) to build the amplifier but as Gemini transistors, i.e. including two dies in the same package, are readily available, this type has been preferred for ease and compactness of building. Moreover, these are better for a perfect amplifier symmetry; their characteristics being closer (matched device) than two independent devices.

The table hereafter includes a list of Gemini transistors (non exhaustive list) capable of at least 200 W RF power.

Reference	Manufacturer	Supply voltage (V)	Output power (W)	Gain (dB)	Efficiency (%)
BLF248	Philips	28	300	13	67
BLF278	Philips	50	300	16	55
BLF368	Philips	32	300	13,5	62
MRF141G	Motorola	28	300	14	55

MRF151G	Motorola	50	300	16	55
D1028UK	Semelab	28	300	13	60
DU28200M	M/A-COM	28	200	13	62
SD2932	STM	50	300	16	60
SR401	Polyfet	28	300	13	55

We chose 28 V operation, as that can easily be achieved by example by putting two 13,8 V power supplies in series, though there are also compact 28 V SMPS (Switched Mode Power Supply) available on the market nowadays. However, in the case one is about to build a dedicated power supply, it should be wise to select a 50 V transistor. These have more gain and are capable of better intermodulation (IMD) behavior. Thanks to its availability and relatively “cheap” price, we selected the **MRF141G**.

3. Theory of operation

The amplifier is based upon a Push-Pull design. It consists of an input 0-180° phase shifter driving two identical active devices working in antiphase. At the output, the same 0-180° phase shifter is delivering the output power of the two active devices to the amplifier load. The phase shifters are actually acting as BALUN (BALANCED-UNbalanced) which transform a balanced system that is symmetrical with respect to ground (the power amplifier itself) to an unbalanced system with one side grounded (here the source, i.e. the transmitter or the load, i.e. the antenna coaxial feeder).

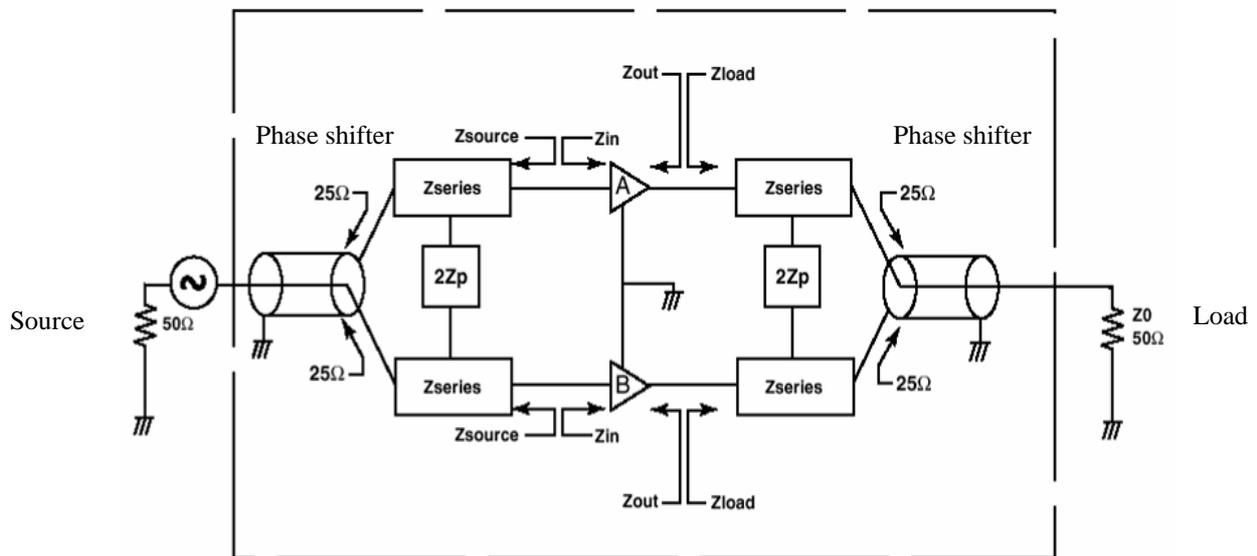


Fig. 1 : Bloc diagram of a Push-Pull amplifier

Starting from the source, the phase shifter delivers on its outputs both 0° and 180° phase shifted components of the input drive signal, together with converting the unbalanced 50 Ω source impedance towards a 2 * 25 Ω balanced impedance. The purpose of the following network (Z_{series} & $2Z_p$) is to transform this 25 Ω into the input impedance (Z_{in}) of blocs A & B, actually the active devices or transistors. Following these transistors, a similar network converts the 2 * 25 Ω balanced impedance of the output phase shifter/Balun so that the transistors are each loaded by

the complex conjugate (Z_{load}) of their output impedance (Z_{out}). In other words, the matching network will force the 25Ω impedance to look like Z_{out}^* to the transistors ($Z_{load} = Z_{out}^*$). The transistors are operated in class B and each of them is alternatively conducting during a half cycle. The output phase shifter/Balun acts the same as the input one but in a reverse way.

4. Design of the amplifier

4.1. MOSFET (Metal Oxide Semiconductor Field Effect Transistor) high-level theory

The transistor used here is a NMOS (N-channel enhancement mode), of which the structure is shown on Fig. 2 below.

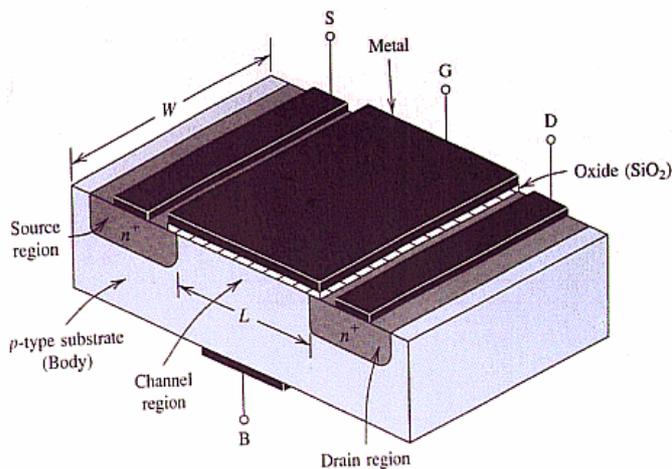


Fig. 2 : Structure of a NMOS

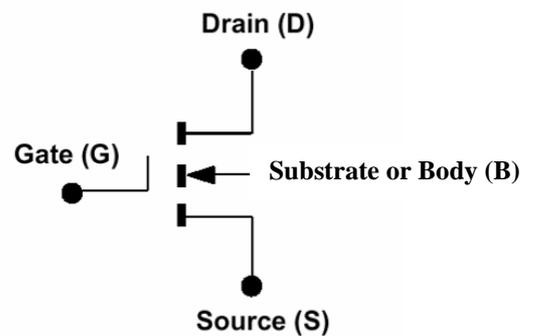


Fig. 3 : Electronic symbol

With a positive (with respect to Source – S) voltage on the Drain (D), the Gate (G) must be biased to a positive voltage (with respect to Source) to allow a Drain-Source current to flow. That biasing then turns on the transistor. This can be seen on Fig. 4.

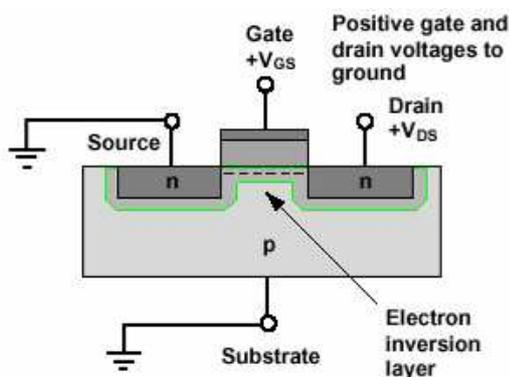


Fig. 4 : Biasing of a NMOS

The minimum value (threshold) of V_{gs} (Gate-Source voltage) which allows a D-S current (I_d) to flow is $V_{gs(th)}$. The value of $V_{gs(th)}$ is controlled during the device

fabrication and typically lies in the range 0,5 to 3 Volts. On the picture below (transfer characteristic), g_{fs} is the Transconductance.

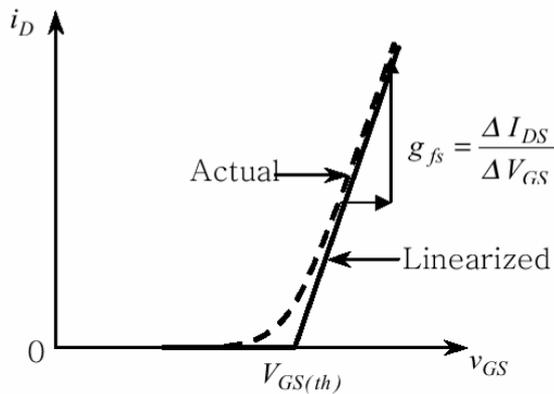


Fig. 5 : Transfer characteristic

4.2. Baluns

The Baluns are made of 50Ω coaxial cable having an electrical length of $\lambda/4$. The outer braid grounded end makes an unbalanced termination while the floating end of the Balun makes a balanced one. Charge conservation requires that the currents on the centre conductor and on the outer braid maintain equal magnitude and a 180° phase difference at any point along the line.

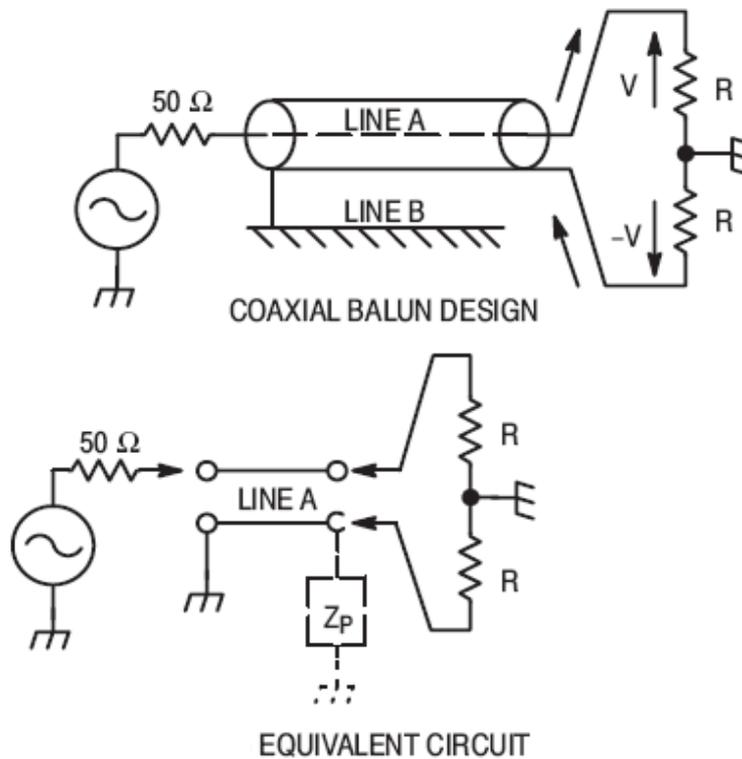


Fig. 6 : Electrical schematic of the Baluns

Knowing the characteristic impedance of the Balun (Z_{Balun}) to be 50Ω , we have :

$$Z_{Balun} = \sqrt{50 * 2 * R} \Rightarrow R = 25 \Omega$$

So, by them-selves, the Baluns are already providing some amount of impedance matching as they lower the amplifier's source & load impedances from 50 to 25 Ω .

Z_p is the parasitic impedance between the floating point of the Balun and the ground. This must be kept as high as possible ($Z_p \gg R$) to avoid an unbalance.

4.3. Input & output impedances

The equivalent schematic of a NMOS is given hereafter (only single-ended device shown) :

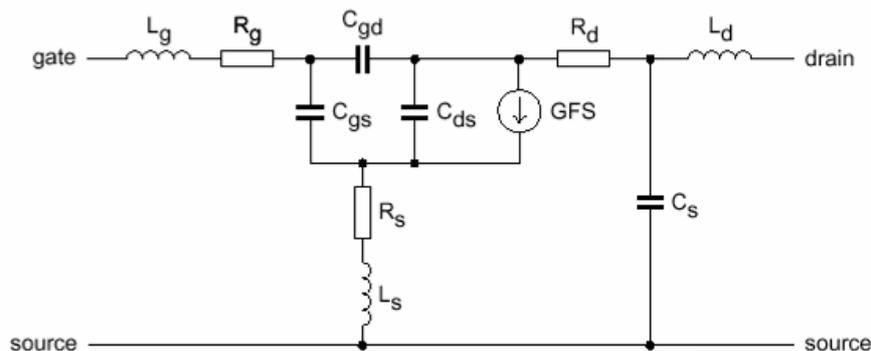


Fig. 7 : Equivalent schematic of a NMOS [1]

For some of the components shown on Fig. 7, the values can be found in data sheets while all of them are embedded in models used by non-linear simulation tools.

Regarding impedance matching, the S parameters are useless here, as these are only valid for small signals, whereas we are operating here in large signal. Nevertheless, the **large signal** input and output impedances of the MRF141G can be extracted from its data sheet (see Appendix 1) :

- $Z_{in} = (R_{in} + jX_{in}) \Omega = (1,20 - j1,50) \Omega$
- $Z_{load}^* = Z_{out} = (R_{out} + jX_{out}) \Omega = (3,90 - j0,85) \Omega$

These are Gate-to-Gate and Drain-to-Drain impedances, for a given operating voltage, bias, frequency of operation and for a particular resistor in parallel with the Gate (which is not often stated in the data sheet).

The impedances are valid for :

- V_{dd} (Drain voltage) = 28 V
- I_{dq} (quiescent current) = 2 * 250 mA (see section 4.5.)
- Frequency = 145 MHz

4.3.1. Input Impedance

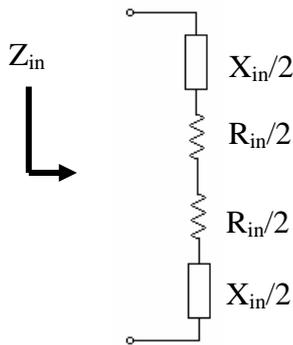


Fig. 8 : Equivalent input impedance Gate-to-Gate

It is assumed the reactance given in the data sheet is a net one, i.e. resulting from both the reactance of the die (capacitive) and the inductive reactance due to the leads and bonding wires of the transistor.

To perform the design, we consider **each side** (or die) of the transistor **individually**

(“half”) and we will calculate the matching circuit for $Z_{in\ half} = \frac{R_{in}}{2} + j \frac{X_{in}}{2}$.

We then consider the input series impedance extracted out of the data sheet :

$Z_{in\ half} (\Omega)$	<i>Equivalent series circuit</i>
$0,60 - j0,75$	$0,60 \Omega + 1,46\text{ nF}$

4.3.2. Output Impedance

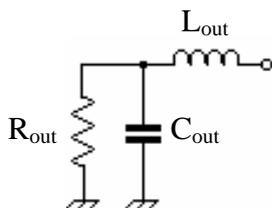
4.3.2.1 First Method

In a similar way as in section 4.3.1., we derive the series output impedance out of the data sheet and, considering one side of the transistor, we get :

$Z_{out\ half} (\Omega)$	<i>Equivalent series circuit</i>
$1,95 - j0,42$	$1,95 \Omega + 2,60\text{ nF}$

4.3.2.2 Second Method

Beside the input & output series impedances given in the data sheet, the equivalent (simplified) schematic of the output impedance of one side (die) of the transistor can be represented as follows :



$$R_{out} = R_{load} = \frac{(V_{dd} - V_{sat})^2}{2 * P_{out}} = \frac{(0,85 * V_{dd})^2}{2 * P_{out}}$$

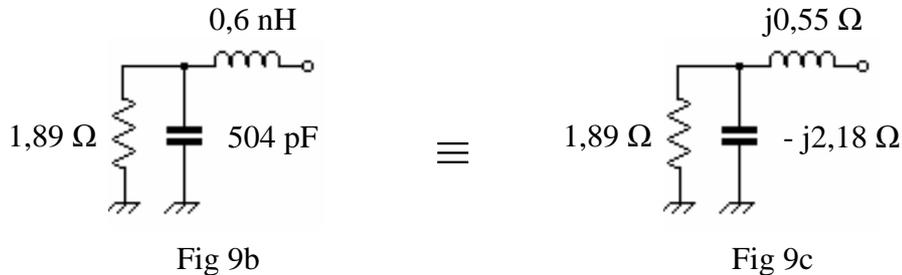
$$C_{out} = 1,2 * C_{oss}$$

$$L_{out} \approx 0,6\text{ nH}$$

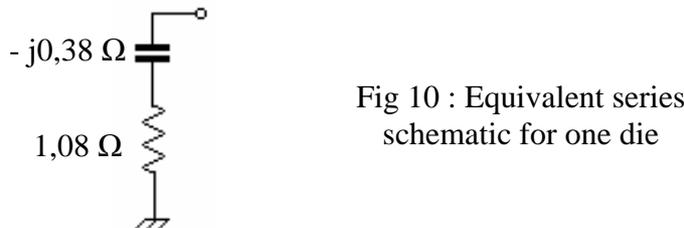
Fig. 9a : Equivalent parallel schematic for one die

$V_{dd} = 28 \text{ V}$, $P_{out} = 150 \text{ W}$ (per transistor/die side) and $C_{oss} = 420 \text{ pF}$ (per die).
 The “1,2” multiplying factor (actually ranging from 1,15 to 1,3) in the calculation of C_{out} is an empirical factor due to the voltage swings that make C_{oss} varying, as indicated in some application notes [1].

L_{out} is assumed from figures found in data sheets and application notes.
 By substituting in the equations, we get :



When using the equations given in Appendix 3 for parallel to series impedance transformation, we can derive the series equivalent schematic :



4.3.2.3 First versus Second Method

As a summary of the two methods, we have :

<i>Method</i>	<i>$Z_{out\ half} (\Omega)$</i>	<i>Equivalent series circuit</i>
<i>First</i>	$1,95 - j0,42$	$1,95 \Omega + 2,60 \text{ nF}$
<i>Second</i>	$1,08 - j0,38$	$1,08 \Omega + 2,89 \text{ nF}$

On a 25Ω normalized Smith Chart, both impedances are relatively close to each other. We will further work here with the second method.

The topic of data sheet impedances, impedances for conjugate match or for best efficiency and S-parameters has been extensively explained in [2].

4.4. Synthesis of the matching networks

Since the transistor input & output impedances have been defined, the task of the designer regarding matching is shown below (still considering one die of the transistor) :

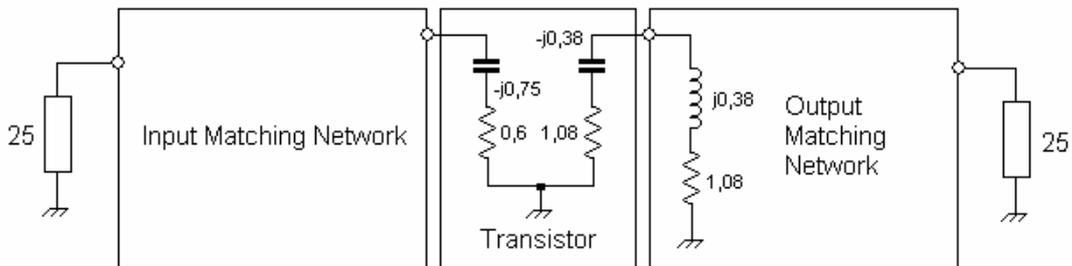
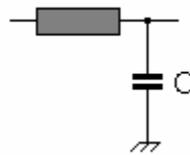
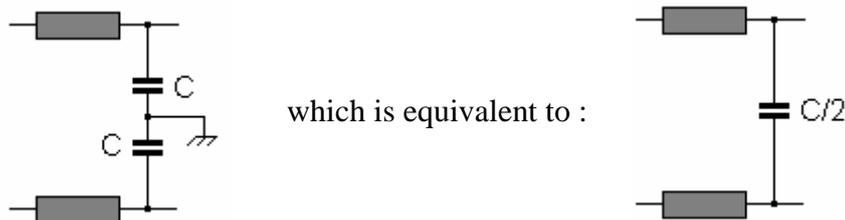


Fig. 11 : Equivalent schematic of the transistor's input & output impedances

The impedance matching networks are made of low-pass filter sections (made of capacitors and printed striplines) :



The two sides of the amplifier will be "merged" as follows :



If the amplifier is well balanced, the currents flowing at the junction of both C capacitors are equal in amplitude and in opposite directions. That point is then acting as a **virtual ground**, so that the ground connection can be omitted and one capacitor (of half value) instead of two can be used.

The matching could be achieved by mean of a single low-pass matching section but this must be avoided. Indeed, we see that the input & output impedances of the transistor are very low, so that a single matching section would require very high Q circuits. High Q will lead to high circulating currents and hence high losses, all together with potential un-stability and too narrow bandwidth circuits. So, the matching is achieved using several cascaded sections.

Though the synthesis of the matching networks can be done graphically “by hand” on a Smith chart, it is more straightforward to use a software. The one used is **Smith V2.03** written by Fritz Dellsperger, HB9AJY [3]. It is here normalized to 25Ω .

There is an infinite number of solutions to “link” 25Ω (center of the chart) from $Z_{in\ half}$ and to $Z_{out\ half}^*$ but always keep in mind a low Q (Q curves can be drawn on the chart) is recommended when choosing the value of the elements. The matching striplines’ characteristic impedance has been set to 25Ω .

4.4.1. Synthesis of the input matching network

The input matching network transforms the transistor input impedance $Z_{in\ half} = (0,6 - j0,75) \Omega$ towards the $(25 + j0) \Omega$ impedance present after the input Balun. In other words, the input matching network makes $Z_{in\ half}$ looking like a $(25 + j0) \Omega$ load to the input Balun.

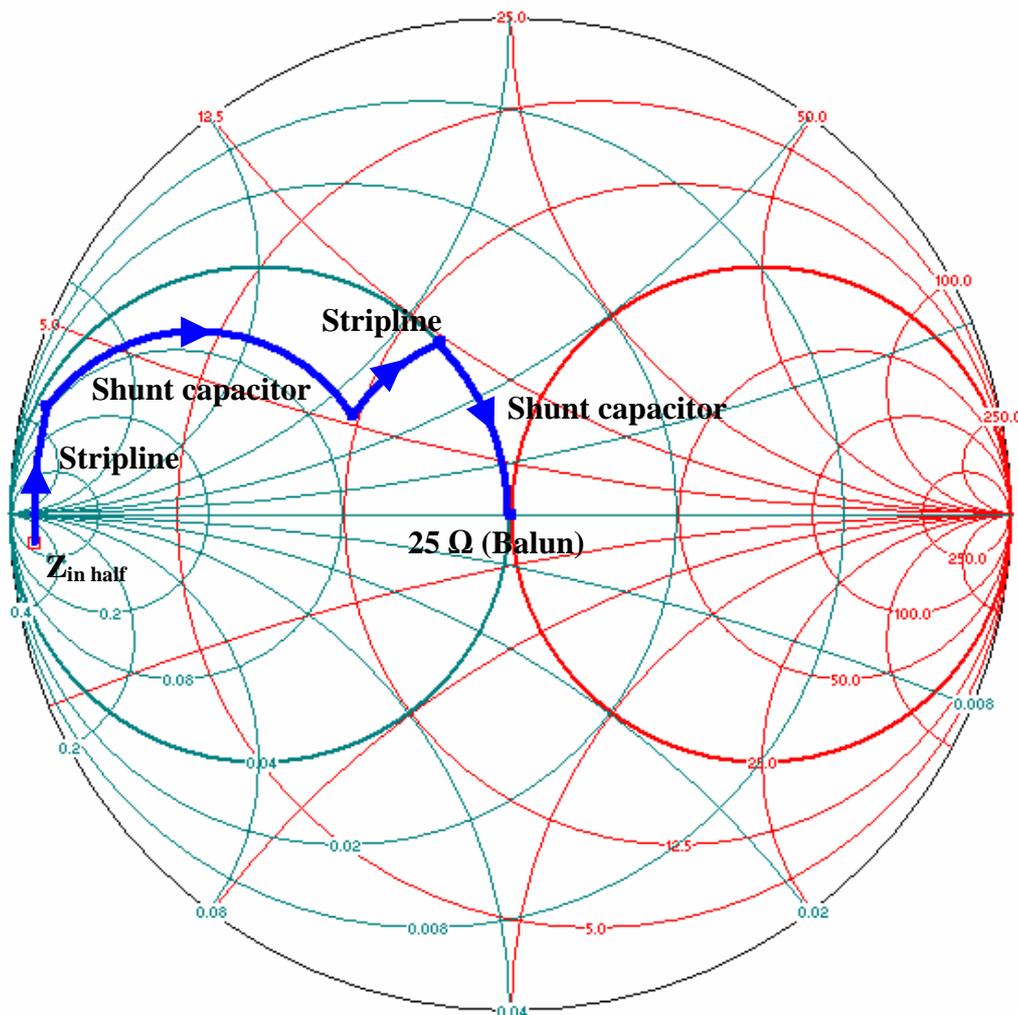


Fig. 12 : Input matching network synthesis on the Smith chart

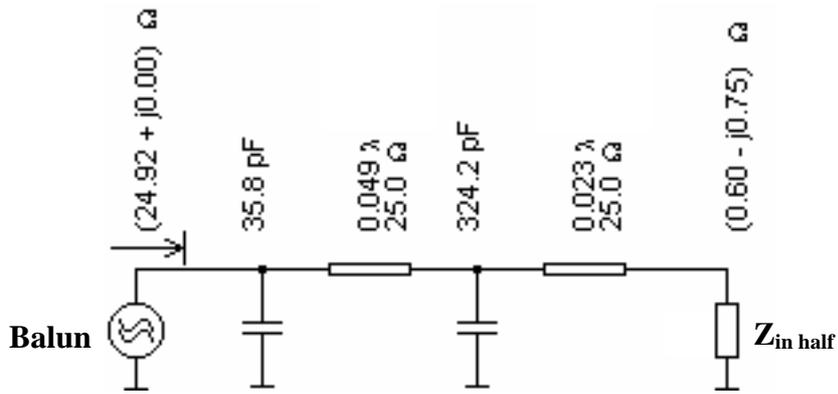


Fig. 13 : Components of the input network (one side)

4.4.2. Synthesis of the output matching network

The output matching network transforms the $(25 + j0) \Omega$ impedance of the output Balun towards $Z_{out\ half}^*$, the complex conjugate of the transistor output impedance. The output matching network forces $(25 + j0) \Omega$ to look like $Z_{out\ half}^*$ to the Drains of the transistor, so that the reactive parts of $Z_{out\ half}$ and $Z_{out\ half}^*$ cancel each others while the resistive parts are equal and provide then the most efficient power transfer.

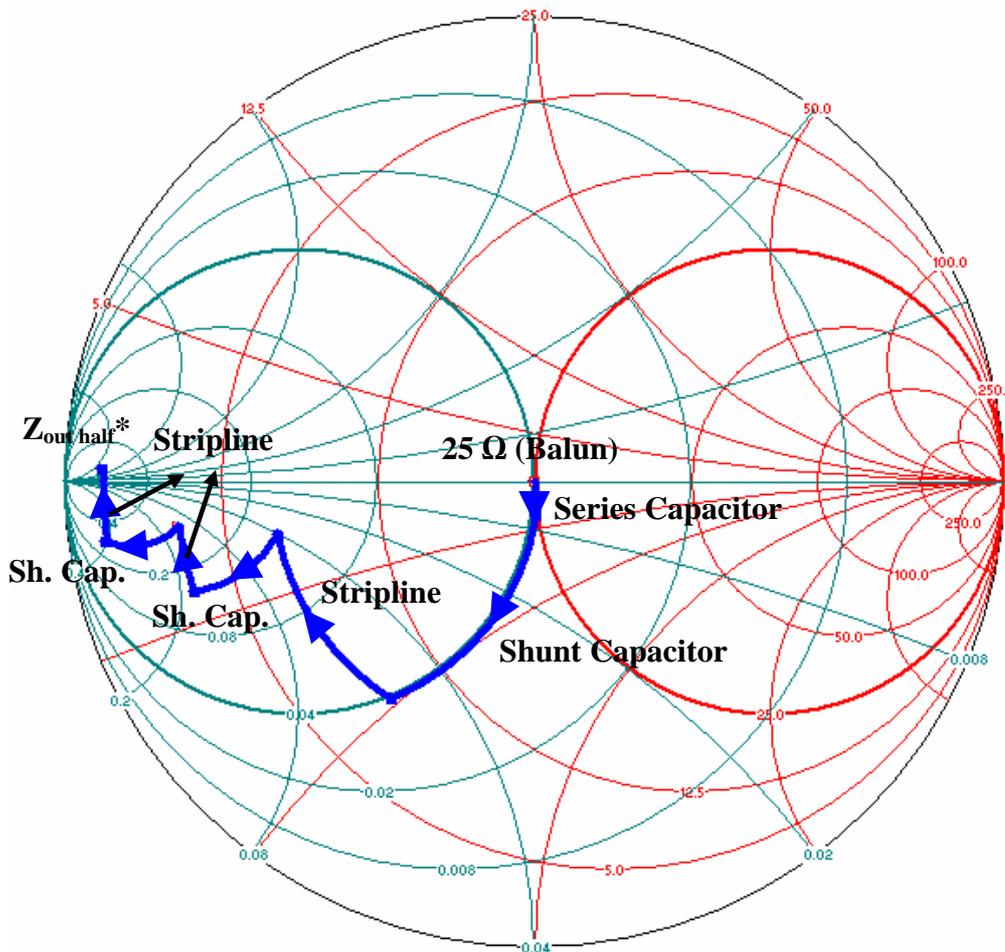


Fig. 14 : Output matching network synthesis on the Smith chart

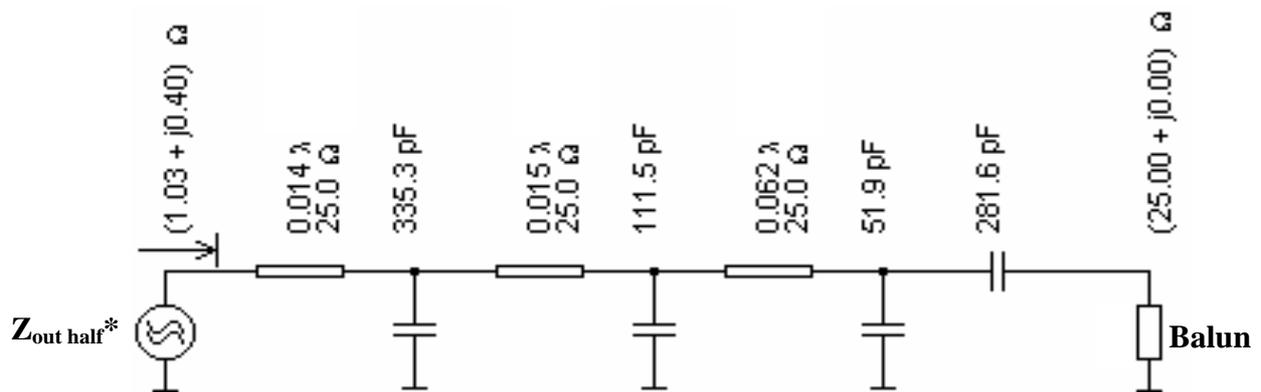


Fig. 15 : Components of the output network (one side)

4.4.3. Comparison between actual and theoretical values

With the theoretical values obtained, the amplifier has been built but at the end, it wasn't delivering the expected output power and was exhibiting an efficiency lower than 50%. So, the component's values have been optimized to increase the output power, the efficiency and the input VSWR. The method used to optimize the values was simply the "cut & try" one...

It is not very scientific but we don't have any mean here to measure the actual transistor impedances nor have access to famous non-linear design software tools. The tables below indicate the differences between the theoretical and actual optimized component's values.

<i>Input Matching Network</i>		
<i>Component</i>	<i>Theoretical value</i>	<i>Actual value</i>
Stripline	0,023 λ	0,023 λ
Shunt Capacitor	324 pF	324 pF
Stripline	0,049 λ	0,057 λ
Shunt Capacitor	36 pF	Variable 44<>76 pF
Shunt Capacitor	-	10 pF @ Balun input (C24 on the RF board part list)

<i>Output Matching Network</i>		
<i>Component</i>	<i>Theoretical value</i>	<i>Actual value</i>
Series Capacitor	282 pF	282 pF
Shunt Capacitor	52 pF	52 pF
Stripline	0,062 λ	0,062 λ
Shunt Capacitor	112 pF	112 pF
Stripline	0,015 λ	0,015 λ
Shunt Capacitor	335 pF	300 pF
Stripline	0,014 λ	0,013 λ

The differences are highlighted in bold. We see that the values of the actually built amplifier are exactly matching or close to the values of the theoretical design.

The difference in the input network can be explained by the fact the damping circuit (see section 4.6.) used for stability purpose introduces new components and hence modifies the impedance. It has also been found experimentally that adding a shunt capacitor of 10 pF in front of the input Balun (C24 on the RF board) improves the input Return Loss.

From a general point of view, if an amplifier is not performing as expected (gain, efficiency, output power) according to the theoretical values of the matching networks' components, the reasons could be :

- Dispersion in the transistor characteristics (different production batches can lead to slightly different impedances, the ones given in the data sheets are average ones).
- Dispersion in the characteristics of the dielectric of the PCB (Printed Circuit Board), mainly impacting the RF tracks (striplines).
- Rounding of the figures on the Smith chart.
- Rounding due to graphical derivation of data out of the data sheets.
- Tolerance of the components.
- According to the class of operation (conduction angle), the value of the load can look different to the transistor (see section 4.5.).
- Quiescent current (I_{dq}), Drain voltage (V_{dd}) and Gate-Source resistor different than the ones stated in the data sheet (if stated).
- Mutual coupling between the striplines (Push-Pull).
- Imperfection of the Baluns.

4.5. Biasing of the amplifier

When operated in class A (small signal), the two dies inside the MRF141G conduct at the same time and the current flowing through each Drain is i .

Given an impedance transformation ratio n (between the Drain and the load), the current flowing in the 50Ω output load (i_L) is :

$$i_L = \frac{2 * i}{n}$$

And the voltage (v_L) across this load is : $v_L = i_L * 50 = \frac{2 * i * 50}{n}$

While the voltage on each Drain is : $v_d = \frac{v_L}{n}$

And the load seen from the Drains is : $R_{dA} = \frac{v_d}{i} = \frac{v_L}{n * i} = \frac{2 * 50}{n^2}$

Operated in Push-Pull class B (large signal), the Drain voltage swing is twice the one of a single-ended class A amplifier. Only one of the two dies inside the transistor package is alternatively conducting (the other being blocked). So, the current flowing in the 50Ω output load is :

$$i_L = \frac{i}{n}$$

And the load seen from the Drains is : $R_{dB} = \frac{50}{n^2}$

We then see that : $R_{dB} = \frac{R_{dA}}{2}$

So, the load seen from the Drains in class B is half the one seen in class A.

From an amplifier gain point (A_V) of view, we have :

$$\text{➤ } A_{V \text{ Small Signal}} = g_{fs \text{ Small Signal}} * R_{dA}$$

$$\text{➤ } A_{V \text{ Large Signal}} = g_{fs \text{ Large Signal}} * R_{dB} = g_{fs \text{ Large Signal}} * \frac{R_{dA}}{2}$$

To be linear, the amplifier must have the same gain for small and large signals. Then :

$$A_{V \text{ Small Signal}} = A_{V \text{ Large Signal}} \Rightarrow g_{fs \text{ Small Signal}} * R_{dA} = g_{fs \text{ Large Signal}} * \frac{R_{dA}}{2}$$

We can conclude : $g_{fs \text{ Small Signal}} = \frac{g_{fs \text{ Large Signal}}}{2}$

The amplifier has then to be biased so that the slope of the transfer characteristic without RF excitation (or $g_{fs \text{ Small Signal}}$) is half the large signal slope ($g_{fs \text{ Large Signal}}$). This avoids crossover distortion, as shown on the following picture :

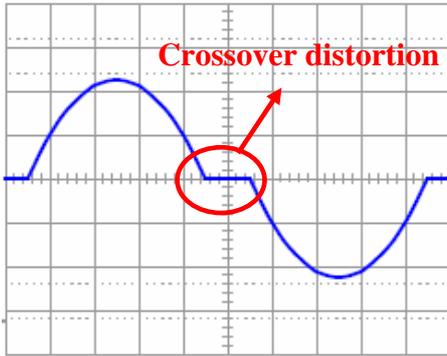


Fig. 16 : Crossover distortion

The goal is then here to set up a Gate voltage (V_{gs0}) so that a quiescent current (I_{dq}) flows through each Drain.

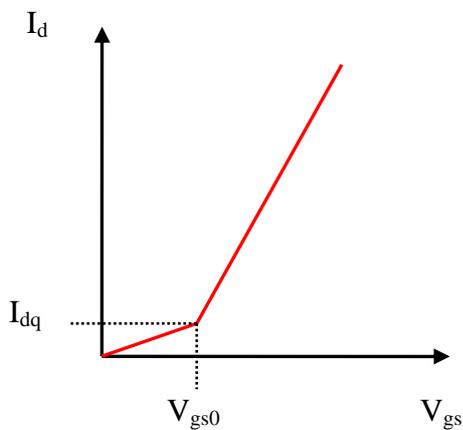


Fig. 17 : Bias point on the transfer characteristic

A MOSFET Gate behaves like a capacitor at DC, thanks to its very high impedance. So, biasing the Gates requires very few current and a simple resistor voltage divider easily fulfils the requirement. Here is an extract from the schematic (see section 5.1.1.) regarding the bias network.

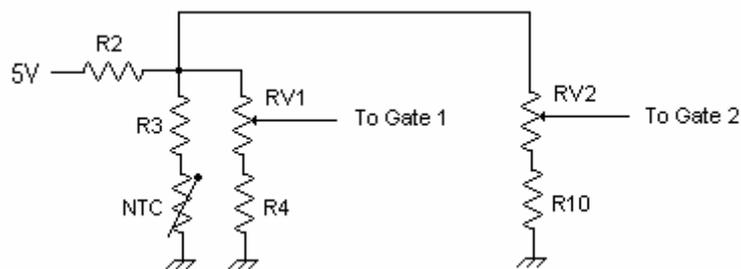
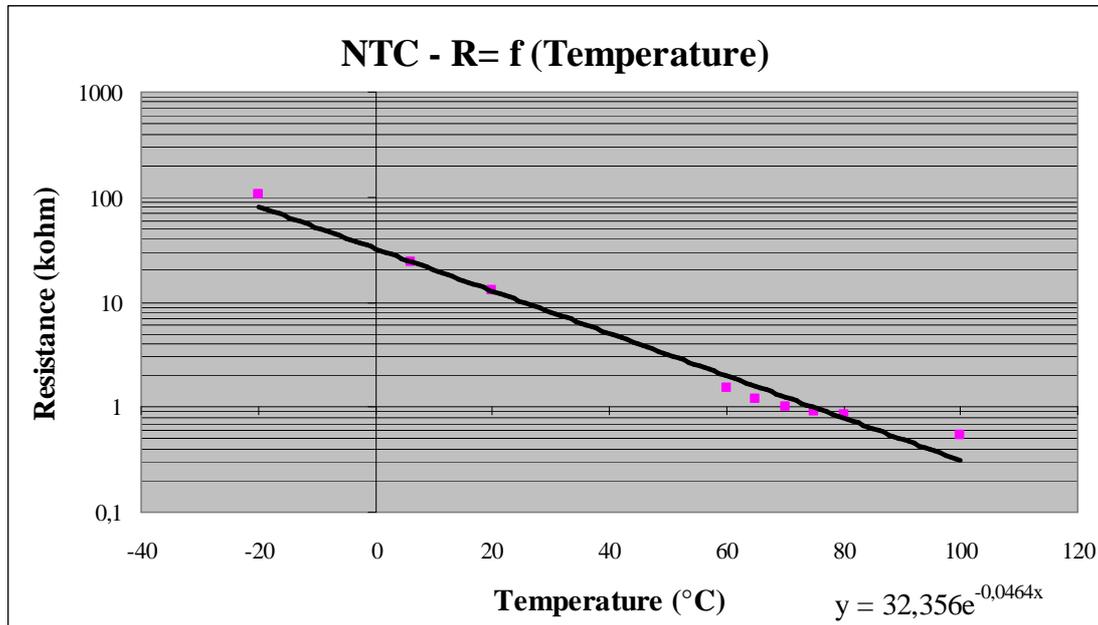


Fig. 18 : Gate bias network

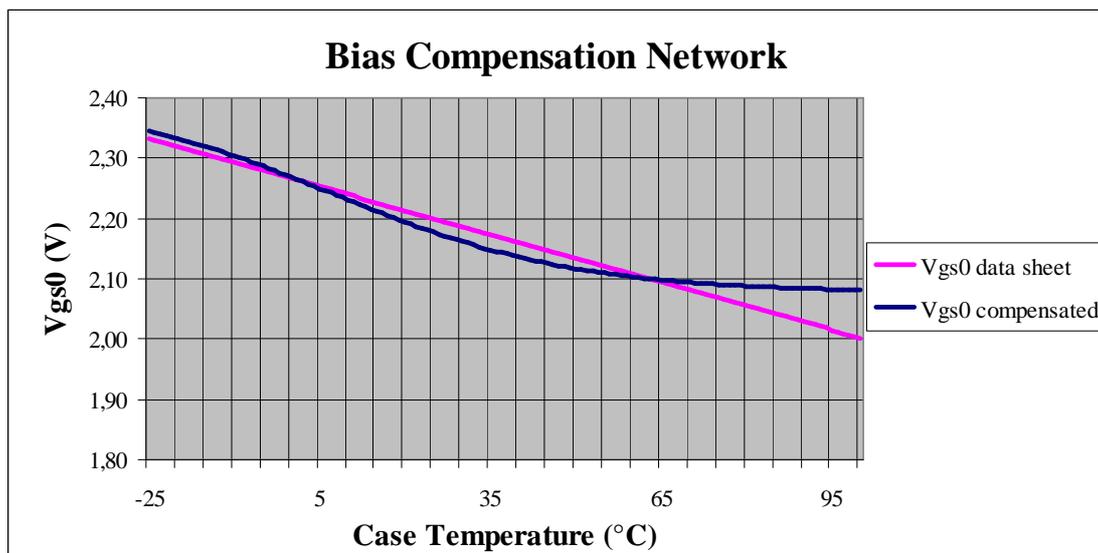
RV1 and RV2 are adjusted to get a quiescent current of 250 mA through each Drain. This is achieved with a V_{gs0} around 2,2 V on each Gate (@ 25°C). Once the (transistor case's) temperature varies, V_{gs0} must be adjusted (compensated) in order to achieve the same quiescent current (I_{dq}) than at 25°C.

The data sheet tells us that the V_{gs0} varies according to the case temperature of the transistor, so that some amount of temperature compensation is needed to keep a

stable bias point. This is achieved by mean of a NTC (Negative Temperature Coefficient resistor). I reused one of my junk-box and unfortunately, it is unmarked. Then, I've measured the value of the NTC according to the temperature; that led to the following graph :



Knowing the value of the NTC according to the temperature and having already fixed the value of all the components but R2 & R3, these last have been calculated (their ratio) so that the compensated V_{gs0} follows the same slope as V_{gs0} in function of the case temperature given in the data sheet. Obviously, both the case of the transistor and the NTC must be in close thermal contact.



4.6. Stability

No particular calculation has been done to assess the stability of the amplifier. Instead, a damping network (R15-C25-C26) has been added at the input (idea extracted from Philips data sheet [4]) and the value of the Gate resistor (R7/R8) has been carefully selected (tested on the amplifier). Both help to damp the Q factor of the impedance matching input network.

With the values shown on the part list of the RF Board, the amplifier is stable, even if its input & output are left open (no load). On the other hand, without any input damping circuit or if the Gate resistor value is above 10 Ω , the amplifier runs into oscillation.

A damping network has been tried at the output of the amplifier but it turned out to be useless.

From a general point of view, the solutions helping in stabilizing a power amplifier are :

- Low Q matching networks (*)
- Damping of matching networks (*)
- Series or parallel Gate resistor (*)
- Drain to Gate feed-back

Three of them (*) are used here.

4.7. Low-Pass Filter (LPF)

A 5 poles LPF has been added at the output of the amplifier to attenuate the harmonics and intermodulation (IMD) products. It is worth to mention here that thanks to the Push-Pull configuration, the even order products (f_1+f_2 , $2f_1+2f_2, \dots$) & even order harmonics ($2f_1$, $2f_2, \dots$) are already well attenuated by the amplifier itself (without filter) if it is well balanced.

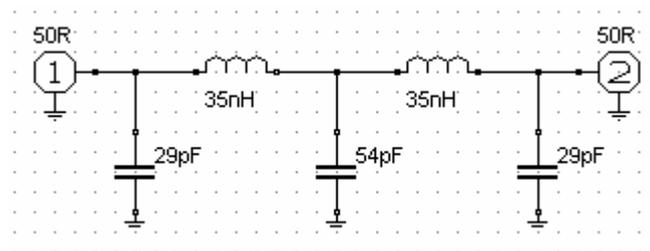


Fig. 19 : Output Low-Pass Filter

The design of the filter has been conducted using the freeware **RFSim99** [5]. The transfer function (S21) and Return Loss (S11) are shown on the graph here after. The simulated filter starts to cut-off a bit above 200 MHz.

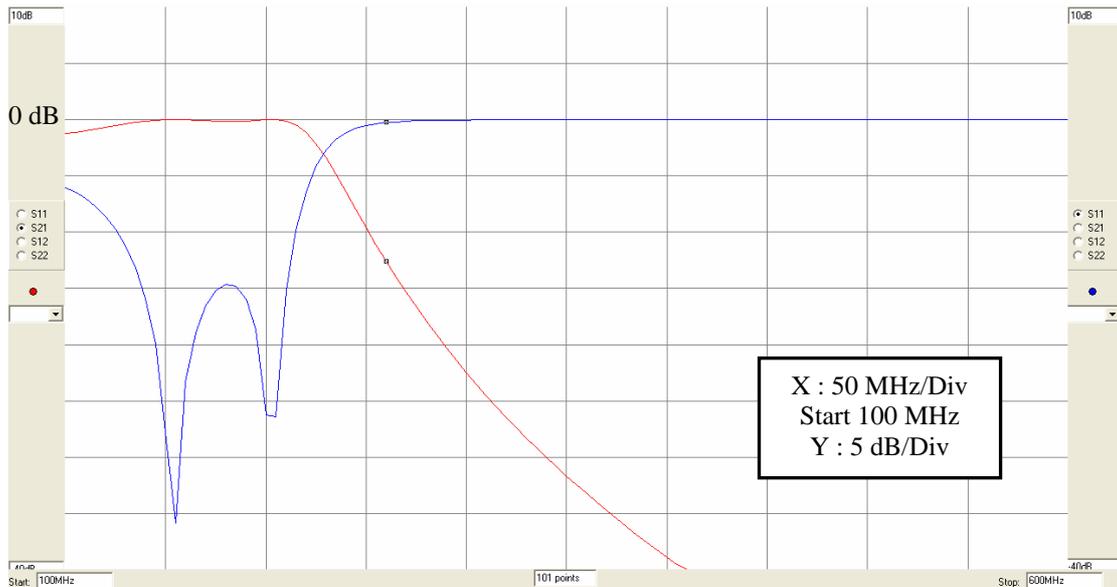


Fig. 20 : Simulated transfer function of the LPF

There would still be room to move the cut-off closer to 150 MHz. However, the measurements done on the built LPF show that the out-of-band rejection is a few dB's better than the simulated one (the effect of the shielded screen between the two inductors was not simulated).

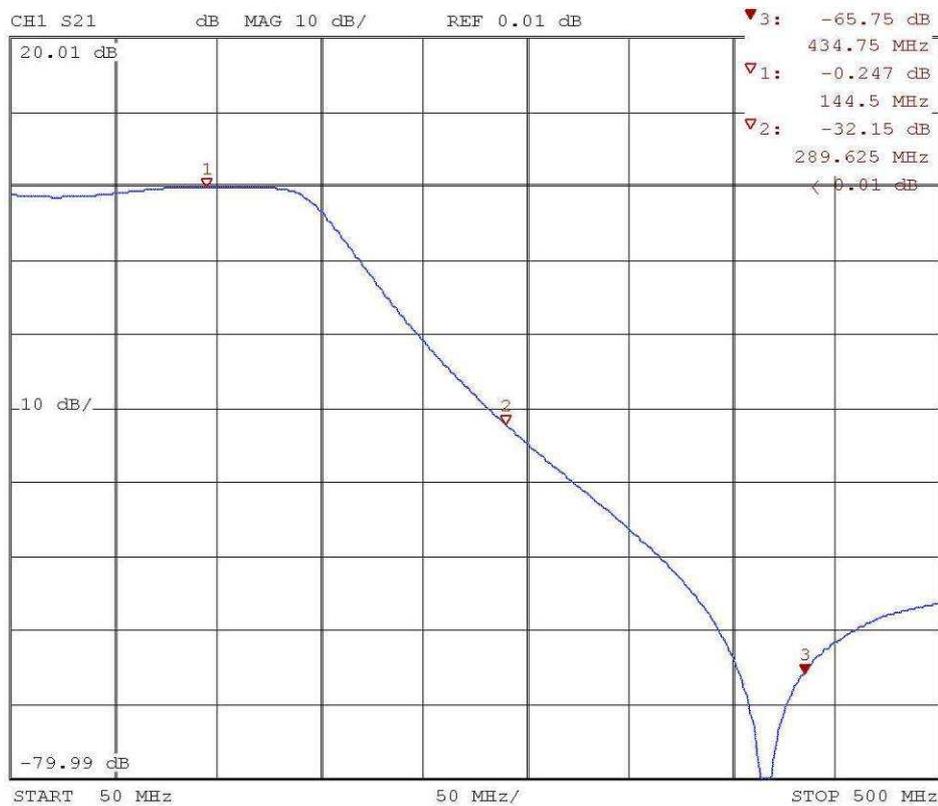


Fig. 21 : Measured transfer function of the LPF

Out of the measurement (Fig. 21), we get the table below :

<i>Frequency</i>	<i>S21 (dB)</i>	<i>Remark</i>
145	- 0,25	Fundamental (f_0)
290	- 32	2 nd Harmonic ($2*f_0$)
435	- 66	3 rd Harmonic ($3*f_0$)
580	- 52	4 th Harmonic ($4*f_0$)

The rejection on the 3rd Harmonic is 66 dB and to avoid degrading this figure by moving the cut-off closer to 150 MHz and hence introducing other self-resonant frequencies by using components of different values, the design has been kept like it is. The Return Loss (S11) is better than 30 dB over the 2m band.

The LPF PCB also includes a basic directional coupler to assess the Direct (Dir.) and Reflected (Ref.) powers for output power monitoring purpose and to supply the VSWR protection circuit. The coupling loss amounts to 30,6 dB on the coupled line.

5. Building of the amplifier

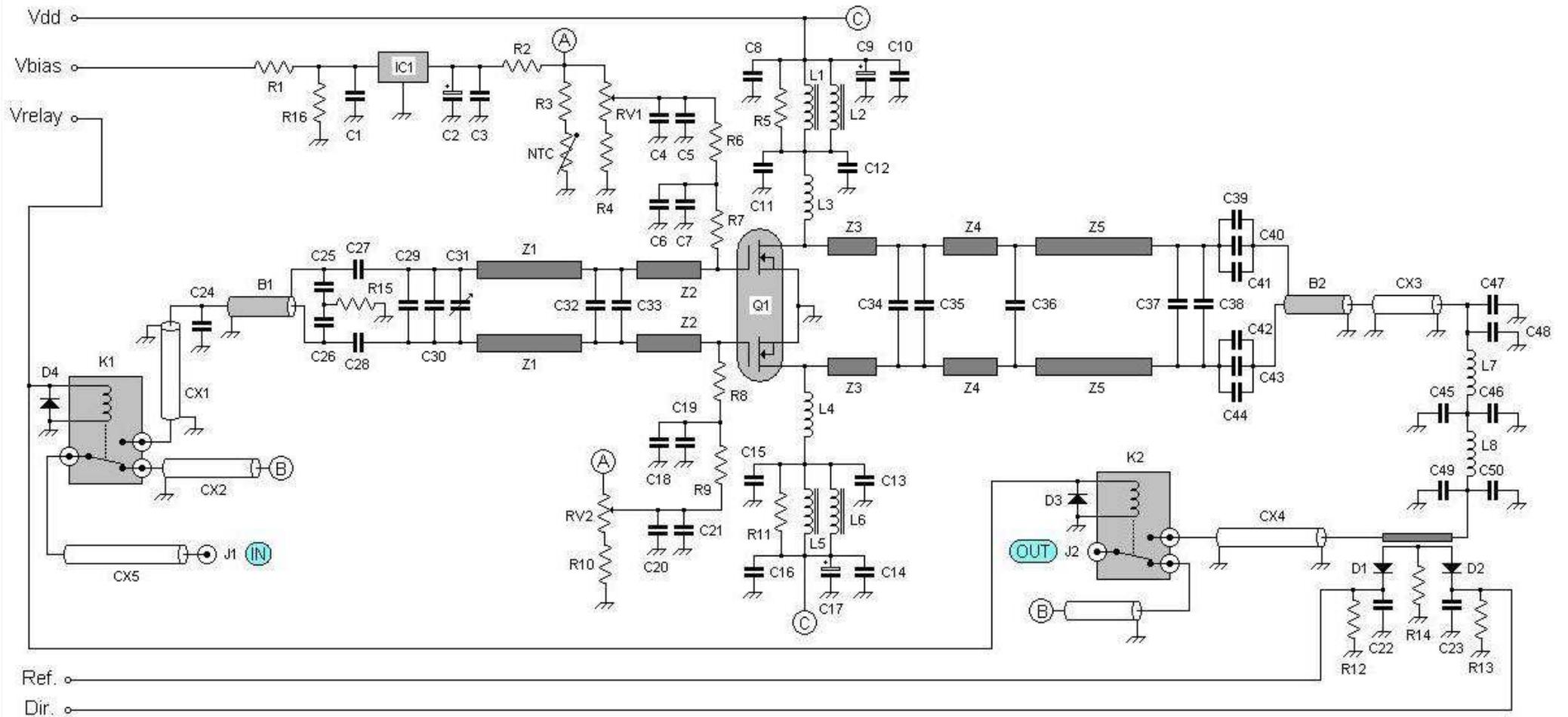
5.1. RF Board

This board actually includes 3 different PCB's, an input PCB, an output one and a small PCB with both the directional coupler and the LPF.

The schematic (see section 5.1.1.) has been drawn with a simple drawing editor (in the present case, MS Paint, part of the MS operating systems). A master file including the most common electronic symbols has been "manually" created.

The schematics are drawn by reusing that same common file and by using the "select" and "copy-paste" functions of MS Paint. Lines are then drawn to link the symbols between each other, while the remaining unused symbols are just deleted.

5.1.1. Schematic of the RF board



5.1.2. Part list

Part ID	Value	Type	Supplier	Remarks
R1	1 k Ω	¼ W	Various	Through Hole
R2	4,7 k Ω	¼ W	Various	Through Hole
R3	20 k Ω	¼ W	Various	Through Hole
R4, R10	10 k Ω	¼ W	Various	SMD 1206
R5, R11	8,2 Ω	1 W	Various	Metal Film MR52
R6, R9	1 k Ω	1,6 W	Various	Metal Film PR37
R7, R8	10 Ω	1 W	Various	Metal Film MR52
R12, R13	1 M Ω	¼ W	Various	SMD 1206
R14	47 Ω	¼ W	Various	SMD 1206
R15	10 Ω	1 W	Various	Metal Film MR52
R16	10 k Ω	¼ W	Various	Through Hole
RV1, RV2	10 k Ω	3314 (¼ W)	Bourns	SMD
NTC	10 k Ω	@ 25°C – See section 4.5.		
C1, C5, C7, C10, C12, C13, C14, C19, C21, C22, C23	1 n	X7R	Various	SMD 1206
C2	1 μ	Tantalum 16V	Various	SMD
C3, C4, C6, C8, C11, C15, C16, C18, C20	100 n	X7R	Various	SMD 1206
C9, C17	10 μ	Electrolytic 50 V	Various	Through Hole
C24	10 p	NP0 500V	Philips	R100G19COGL (1)
C25, C26	27 p	P100 Porcelain	Temex (Hi-Q)	500CHB270FV
C27, C28	1 n	P90 Porcelain	ATC (100B)	ATC100B102KW500
C29	4,7 p	P100 Porcelain	Temex (Hi-Q)	500CHB4R7BV
C30	15 p	NP0 500V	Philips	R150G19COGL
C31	2-18 p	PTFE dielectric film	Philips	2222 809 05217
C32	150 p	P90 Porcelain	ATC (100B)	ATC100B151JW500
C33	12 p	P100 Porcelain	Temex (Hi-Q)	500CHB120FV
C34, C39, C44	82 p	P100 Porcelain	Temex (Hi-Q)	500CHB820FV
C35	68 p	P100 Porcelain	Temex (Hi-Q)	500CHB680FV
C36	56 p	P100 Porcelain	Temex (Hi-Q)	500CHB560FV
C37	18 p	P100 Porcelain	Temex (Hi-Q)	500CHB180FV
C38	8,2 p	P100 Porcelain	Temex (Hi-Q)	500CHB8R2BV
C40, C41, C42, C43	100 p	P100 Porcelain	Temex (Hi-Q)	500CHB101FV
C47, C50	6,8 p	P100 Porcelain	Temex (Hi-Q)	500CHB6R8BV
C48, C49	22 p	P100 Porcelain	Temex (Hi-Q)	500CHB220FV
C45	15 p	P100 Porcelain	Temex (Hi-Q)	500CHB150FV
C46	39 p	P100 Porcelain	Temex (Hi-Q)	500CHB390FV
L1, L2, L5, L6		VK200 Choke	Philips	
B1, B2		$\lambda/4$ Balun	Home	See section 5.1.3.
D1, D2	5082-2811	Schottky	Agilent (HP)	Through Hole
D3, D4	1N4148		Various	Through Hole

Q1	MRF141G		Motorola, Tyco Electronics, M/A-Com	(2)		
IC1	7805	5V Regulator	Various			
CX1, CX2, CX3, CX4, CX5	RG 400	Coax cable sections	Huber&Suhner			
K1	CX120A	Coax Relay	Tohtsu			
K2	CX520D	Coax Relay	Tohtsu			
J1	Female N	Connector	Various	On Front-Panel		
J2	Female N	Connector	Various	Part of K2 (CX520D)		
Homemade Inductors' data						
	Value	Internal Ø	Wire Ø	Length	Winding	# Turns
L3, L4	≈ 35 nH	5 mm	1,5 mm	17 mm	Spaced	4,5
L7, L8				14 mm, mounted 5 mm above PCB		3,5
Striplines' data						
	Length (mm)	Width (mm)	El. Length (λ)	Remarks		
Z1	61,0	7,5	0,057	0,3mm th., 5mm wide CuAg strip soldered on PCB's stripline		
Z2	23,5		0,023			
Z3	14,0		0,013			
Z4	16,0		0,015			
Z5	68,0		0,062			
PCB's : 1,6 mm thick, double sided FR4 epoxy glass fiber (ε_r = 4,6)						

(1): Experimentally, it has been found this capacitor improves the input Return Loss.

(2): Can be bought at RF Parts (<http://www.rfparts.com>) in the USA. ASI Advanced Semiconductor Inc is also selling the MRF141G (<http://www.advancedsemiconductor.com>).

5.1.3. Baluns

The input Balun is made of RG 316 PTFE dielectric 2,5 mm O.D. coaxial cable manufactured by H&S. The output Balun is made of RG 400 cable of the same manufacturer. The velocity factor (V_f) of both types of cable is 0,695.

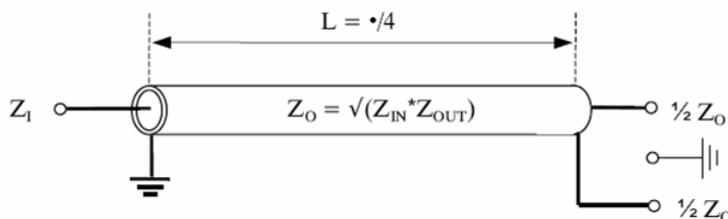


Fig. 22 : Drawing of the Baluns

Both cables have an electrical length of $\lambda/4$ and a characteristic impedance of 50 Ω.

This leads to a physical length of $\frac{300}{145} * 0,25 * V_f = 36 \text{ cm}$

Make them a little bit longer to allow the solder junctions with the matching striplines. Both Baluns are wound as shown on the pictures (see section 8). The winding diameter amounts to around 50 mm.

As can be noticed on the same pictures, $\lambda/8$ printed Baluns with semi-rigid cable have been initially used but without too much success.

Note : H&S is no more manufacturing the RG 316 & RG 400 but the Enviroflex 316 & 400 instead. These have slightly different characteristics.

5.1.4. Matching striplines & PCB's

The 3 PCB's of the **RF Board** are made of **1,6 mm thick double sided FR4 epoxy glass fiber ($\epsilon_r = 4,6$)**. Apart from the RF tracks, the layout is not critical.

The 2 sides of the PCB's are linked together by Cu strips (Cu foil is easily available from the external "braid" of a piece of H100 coax cable) all around the PCB's and by as many vias as possible. Moreover, the input and output PCB's are also linked together by Cu strips each sides of the transistor. The pictures of section 8 are self-explanatory.

When it is all about high currents and low impedances, ground continuity is very important, also for stability of the amplifier.

All PCB's are screwed directly onto the heat sink.

The striplines have been designed thanks to the freeware **AppCAD** [6] of Agilent. Here is an example :

The building data of the critical RF tracks are shown on the pictures below :

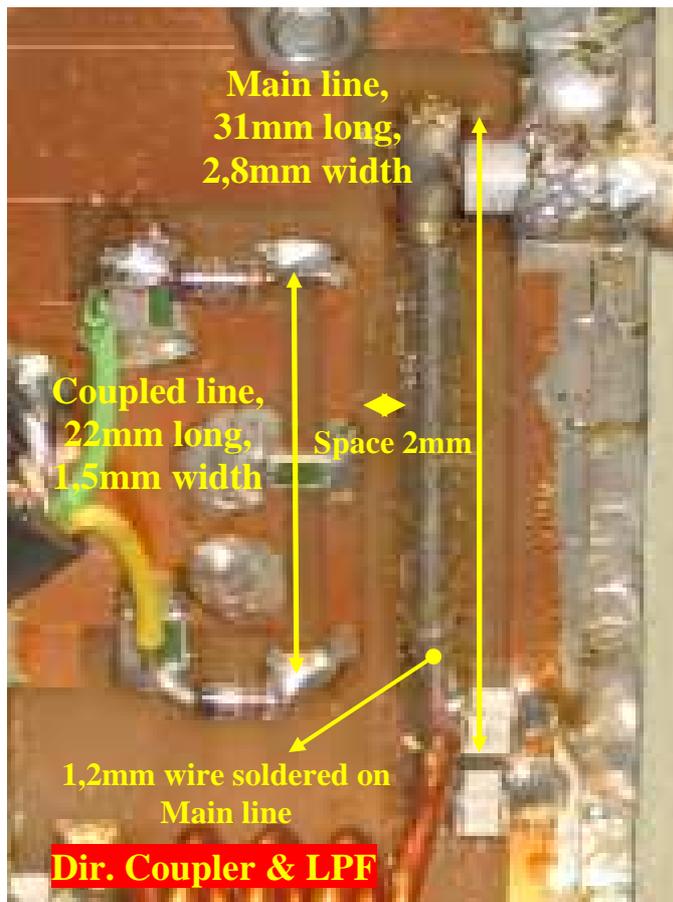


Fig. 23 : Directional coupler RF tracks details

5.1.5. Cooling

The heat sink has been recuperated from a military surplus power supply (see pictures in section 8). No heat transfer calculation has been done, but the heat sink turned out to be big enough to allow SSB/CW operation without any extra cooling mean (at room temperature). When the weather is hot (remember, the amplifier is operated “Outside”, of course protected against rain but in a non air-conditioned environment) or for heavy duty operation (digital modes), a snail blower cools the amplifier down; it provides more than enough cooling. Even during long periods of operation, the heat sink stays at room temperature.

The transistor is screwed on a thin (1 mm thick) Cu piece, acting as a heat spreader, itself in close contact (screwed) with the heat sink (made of aluminum). Some heat conducting compound is used too.

To avoid mechanical stress due to temperature changes, it is recommended to bend the transistor leads, though it hasn't been done here. The transistor leads have been kept straight and soldered as such on the PCB's.

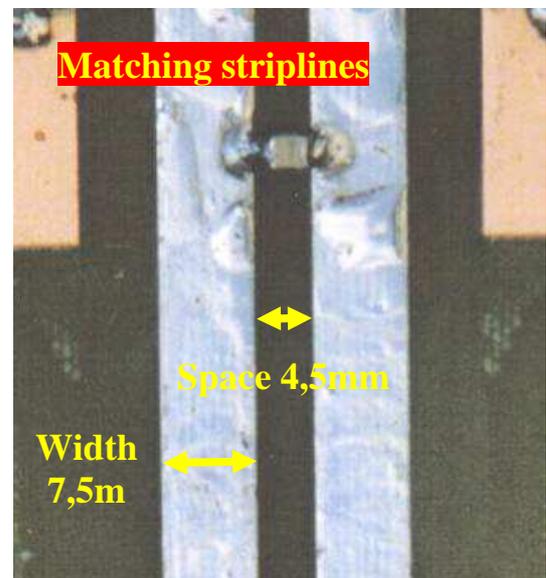


Fig. 24 : Matching striplines details

5.2. Control board

This board supervises the amplifier. It has been mounted on a **perforated board** onto which there are holes/Cu pads each “e” (1 e = 2,54 mm).

Once S1 (front-panel) is set to “ON” and S2 (front-panel) to “Operate”, the amplifier is ready to operate. When the PTT (front-panel) input is grounded, the amplifier goes to TX mode; this is indicated by the D5A red LED, lighting on the front-panel. The amplifier is sequenced to avoid “hot” switching of the coax relays. Indeed, RV2 and C7 introduce a time delay so that the bias is applied to the transistor **AFTER** the K1 & K2 coax relays (RF Board) have been switched to TX (Normally Open position of the coax relays). In RX, it is the D5B green LED that lights on the front-panel.

The Operational Amplifiers IC2A and IC2D shape the “reflected” voltage out of the directional coupler (LPF PCB) to drive the TH1 thyristor that is the heart of the VSWR protection circuit. RV3 sets the VSWR threshold as from which the amplifier goes into protection. Once in protection, the bias is disabled and the coax relays go back to Normally Closed state (RX mode). The amplifier remains in protection mode until the “Reset” push button (front-panel) is pressed (after the fault in the antenna line has been found and fixed). IC2B amplifies the voltage sampled out of the direct power by the directional coupler. This voltage, proportional to the output power, could be displayed on the front-panel meter but instead, a “Monitor” output on the front-panel is used on my device. So, the proper working of the amplifier can be monitored remotely (in the shack, 50 m away from the amplifier location) by mean of a LED (not shown on the schematic) that lights according to the RF output power level. In place of just a LED, a (Volt-)meter can of course also be used. RV4 sets the maximum voltage on the “Monitor” output.

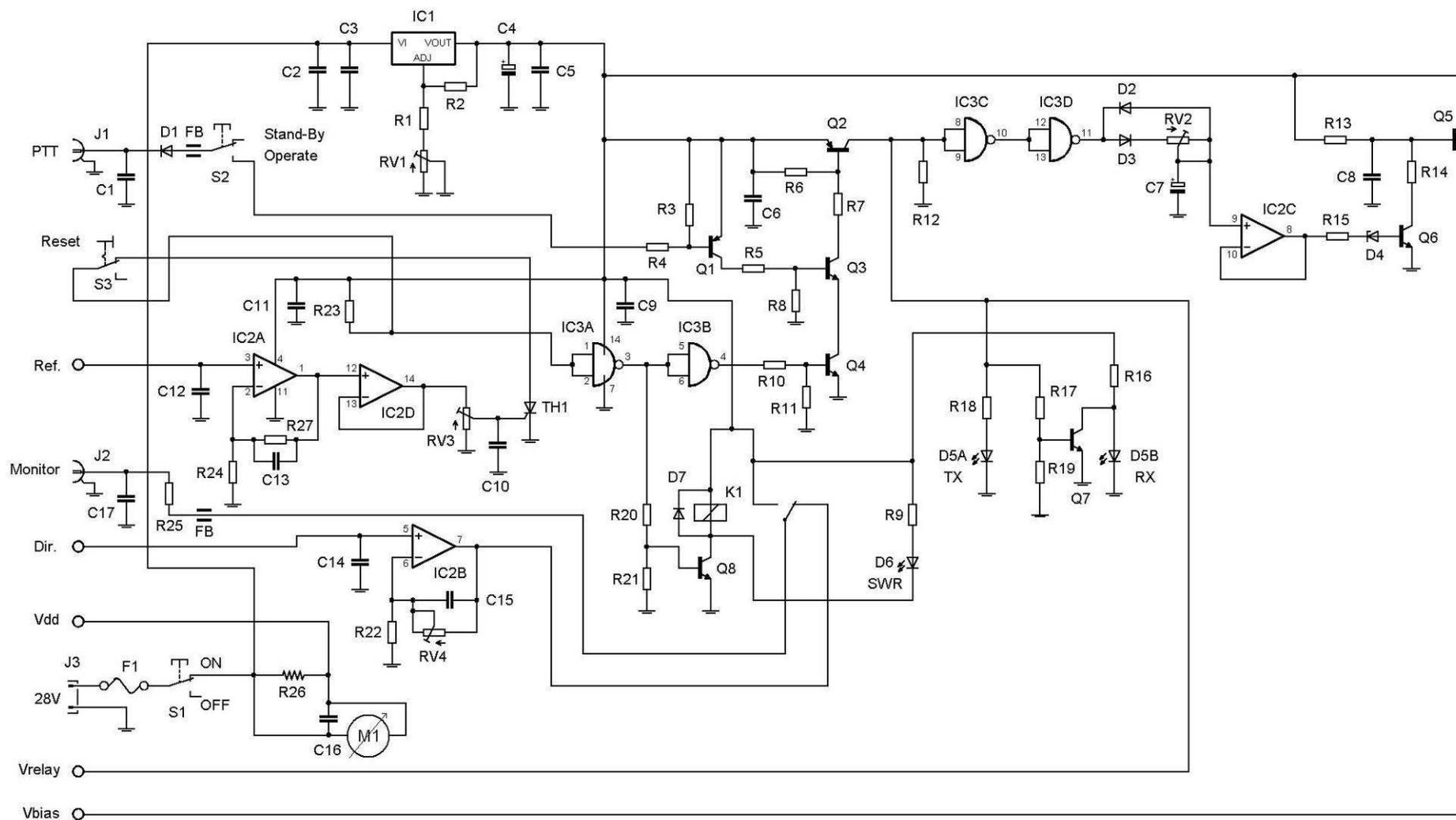
If due to bad VSWR the amplifier goes into protection, the relay K1 switches, so that the monitor voltage goes to high state until the “Reset” button is pressed. This can be used to activate an alarm. In the present case, both the remote monitoring and the front-panel (D6) LED’s light at full bright in case the amplifier goes into protection.

The **VSWR protection is mandatory**, the transistor can handle a 5:1 VSWR but a short or an open in the antenna line makes the VSWR to be infinite...

R26 is a shunt resistor (75 mV drop under 30 A) that, together with the M1 meter, indicates (on the front-panel) the total Drain current drawn by the transistor.

The schematic here has been drawn with **EAGLE Light Edition** [7].

5.2.1. Schematic of the Control board



5.2.2. Part List

As this is a low frequency board, the package type of the components (through hole or SMD) is not critical. It is then not mentioned in the table below.

Part ID	Value	Type	Supplier	Remarks
R1	1,6 kΩ	¼ W	Various	
R2	237 Ω	¼ W	Various	Tolerance 1%
R3, R4	3,3 kΩ	¼ W	Various	
R5, R15, R17, R20, R21	2,2 kΩ	¼ W	Various	
R6, R8, R11, R19	10 kΩ	¼ W	Various	
R7, R9, R14, R18	1 kΩ	¼ W	Various	
R10, R13	4,7 kΩ	¼ W	Various	
R12	47 kΩ	¼ W	Various	
R16, R23, R25	820 Ω	¼ W	Various	
R22	220 kΩ	¼ W	Various	
R24	100 kΩ	¼ W	Various	
R26	2,5 mΩ	Shunt Resistor, 75 mV drop under 30 A		
R27	1 MΩ	¼ W	Various	
RV1	2,2 kΩ	½ W	Various	
RV2	50 kΩ	½ W	Various	
RV3	10 kΩ	½ W	Various	
RV4	1 MΩ	½ W	Various	
C1, C2, C6, C8, C9, C10, C11, C12, C13, C14, C15, C16, C17	1 n	X7R	Various	
C3, C5	100 n	X7R	Various	
C4	15 μ	Electrolytic 50 V	Various	
C7	1 μ	Tantalum 16V	Various	
D1, D2, D3	1N4148		Various	
D4	9,1 V	BZX79C Zener diode	Philips	
D5	Dual color LED	Red/Green	Various	On Front-Panel
D6	LED	Red	Various	On Front-Panel
TH	2N5064	Thyristor	Various	
Q1	2N2907	PNP	Various	
Q2	BD676	Darlington PNP	Various	
Q3, Q4, Q6, Q7, Q8	BC109	NPN	Various	
Q5	2N2904	PNP	Various	
IC1	LM317T	Volt. regulator	Various	
IC2	LM324	AOP	Various	
IC3	HEF4011BD	NAND gates	Various	
K1	DO12-M	12V relay	Fujitsu	Any small relay is OK
S1	Switch	SPDT	Various	10 A handling, Front-Panel

S2	Rotary switch	At least 2 positions	Various	On Front-Panel
S3	Push button	Norm. Closed	Various	On Front-Panel
M1		Drain current meter	Various	Sold with shunt resistor (R26) – 6,8 mA for full scale deviation, 11 Ω internal resistor
F1	25A	Car fuse	Various	
J1, J2	RCA Jack	Connector	Various	On Front-Panel
J3		Power Connector	Various	On Front-Panel
FB	Ferrite bead		Various	
PCB : perforated board				

6. Commissioning

This section describes the steps to be completed in order to set the amplifier up and running.

1. Set RV1 of Control board so that its hot end (the one linked with R1) is set to ground.
2. Set RV1 & RV2 of RF board so that the cursor is set to cold ends (the ones linked with R4 & R10). Short-circuit R4 & R10 of the RF board to ground (the MRF141G is blocked).
3. Set the cursor of RV3 of the Control board to the cold end (ground).
4. Slowly adjust RV1 (Control board) to get 13 V at the output of the LM317 (IC1). Be careful not to exceed 15 V for the safety of IC3.
5. Without any RF drive applied, set the PTT input on the front-panel (J1 of Control board) to ground back and forth while adjusting RV2 of the Control board so that V_{bias} (collector of Q5 on the Control board) arises **AFTER** the coaxial relays have been switched.
6. Disconnect CX3 from the amplifier's output PCB of the RF board and terminate it with a $50\ \Omega$ load (min 10W). Mechanically switch K2 (to Normally Open position) of the RF board and inject 8W of RF power on J2 (front-panel) of the RF board. Then, adjust RV3 of the Control board so that the front-panel "SWR" LED (D6) lights. This settles the VSWR protection threshold. At full output power (300W), a reflected power of 8W corresponds to a 1,4:1 VSWR.

Remove the $50\ \Omega$ load and re-connect CX3 on the output PCB of the RF board.

7. Load J2 (front-panel) of the RF board with a high-power $50\ \Omega$ load ($> 300W$) through a Watt-meter. Connect a transceiver to J1 (front-panel) of the RF board through a VSWR/Watt-meter. Link the transceiver's PTT to J1 (front-panel) of the Control board. Set the transceiver power to 3W and key it. Adjust C31 of the RF board (with an isolated screwdriver) to achieve the best possible input VSWR while checking the output power. Around 100W of output power must be obtained. Raise slowly the transceiver power while re-adjusting C31 to keep on a good input VSWR. The worst Return Loss (VSWR) is 18 dB at mid drive power; at low and full drive, the VSWR-meter needle doesn't deviate at all.

With 13W of drive power, the output power should lie around 300W, together with achieving a 50% efficiency. Below 300W, it is normal that the efficiency is worse. Due to the dispersion of the characteristics of the components (compared to the ones used here), the perfect matching won't probably be achieved at first try. Extra tuning of the capacitors being part of the matching networks would then be required. This will be achieved by temporarily soldering variable capacitors instead of, or in parallel with the ones already in place. Capacitors of the same type as C31 will do the job.

Tuning is an iterative process. Start at low drive power levels and tune the output matching network, from the transistor to the output, back and forth. Then, tune the input network the same way. Afterwards, come back on retuning the output network. And so on at different drive levels up to the maximum is reached.

8. Adjust RV4 of the Control board to obtain the wanted monitor voltage (proportional to the output power) on J2 (front-panel) of the Control board.

7. Performance

Due to lack of measurement tools, the performance assessment has been quite limited. However, at least the output power has been measured, as seen hereafter :

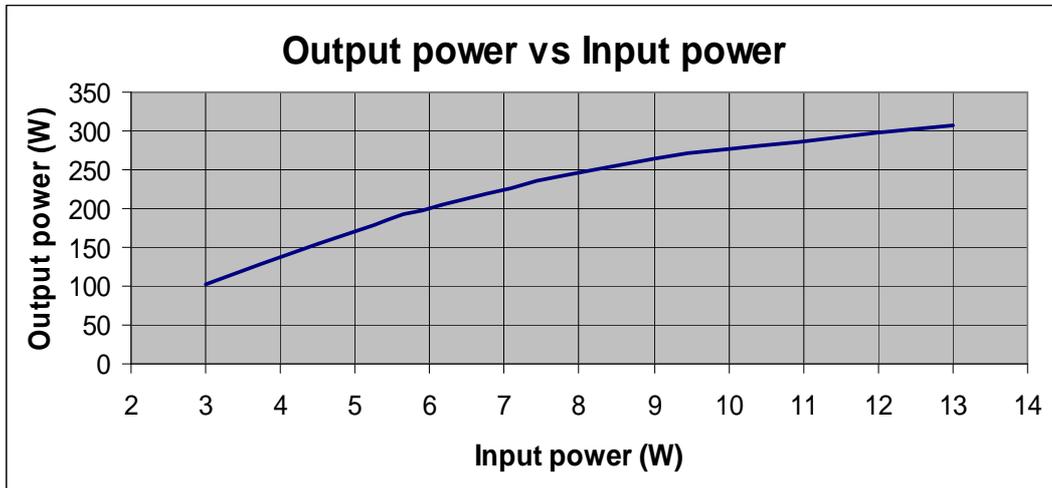


Fig. 25 : Output power versus input power

The mean **gain is 15 dB** and the **1 dB compression point** lies at **280W** output power. Though the level of the intermodulation products and harmonic rejection hasn't been measured, the following picture, extracted from a Motorola application note [8], shows the harmonic rejection of a **broadband** amplifier using the MRF141G. One clearly sees that at low frequency, the amplifier output shows an even harmonics content already well rejected (without any LPF) by the amplifier of its own, while the level of the odd harmonics remains quite high. However, at 144 MHz, the worst harmonic level is -45 dBc (third harmonic). Assuming the amplifier described here behaves the same way than the broadband one (which is unlikely to occur, thanks to the narrowband nature of the present amplifier, of which matching networks are made of LPF sections) and given the additional rejection provided by the output LPF, a **minimum** (theoretical) **harmonic rejection of 77 dBc** can be expected (for all orders).

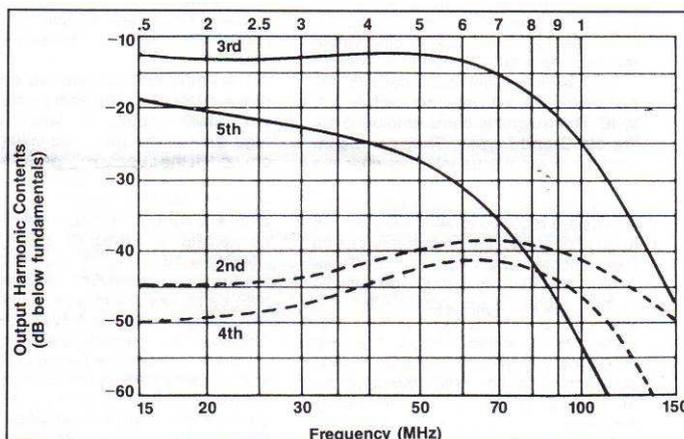


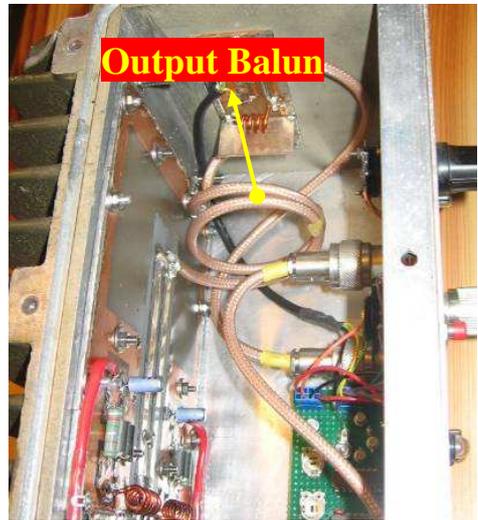
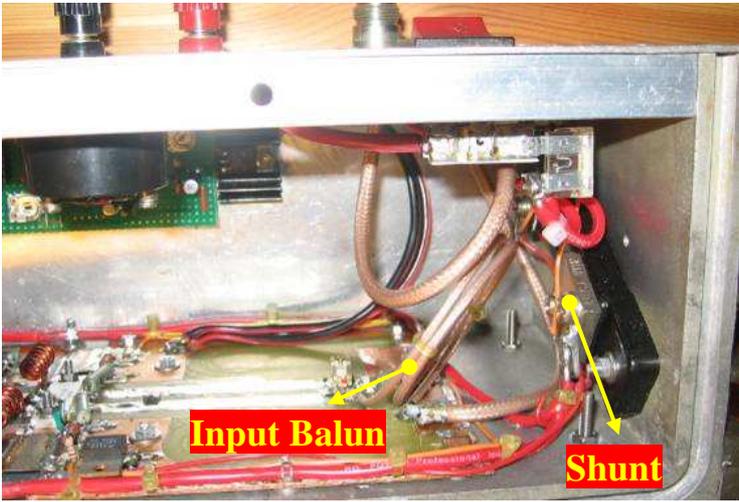
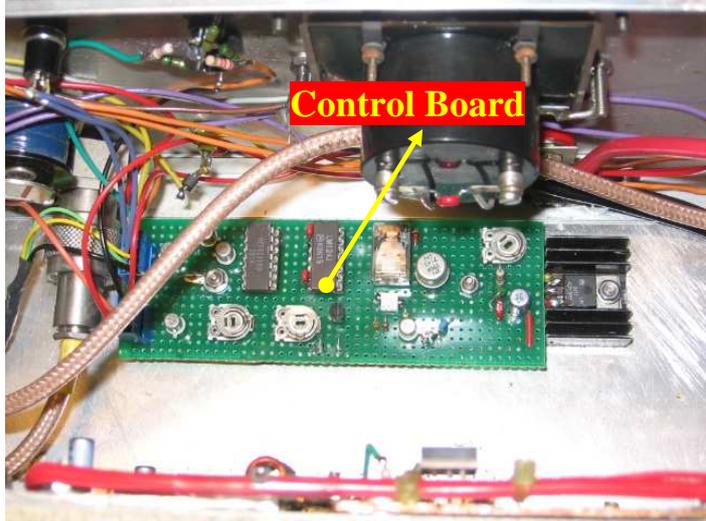
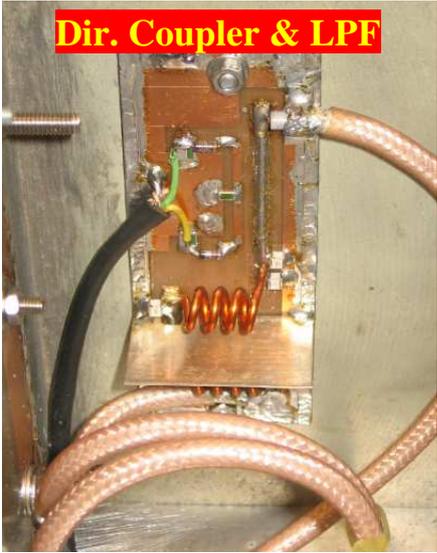
Fig 26 : Harmonic content of a broadband MRF141G

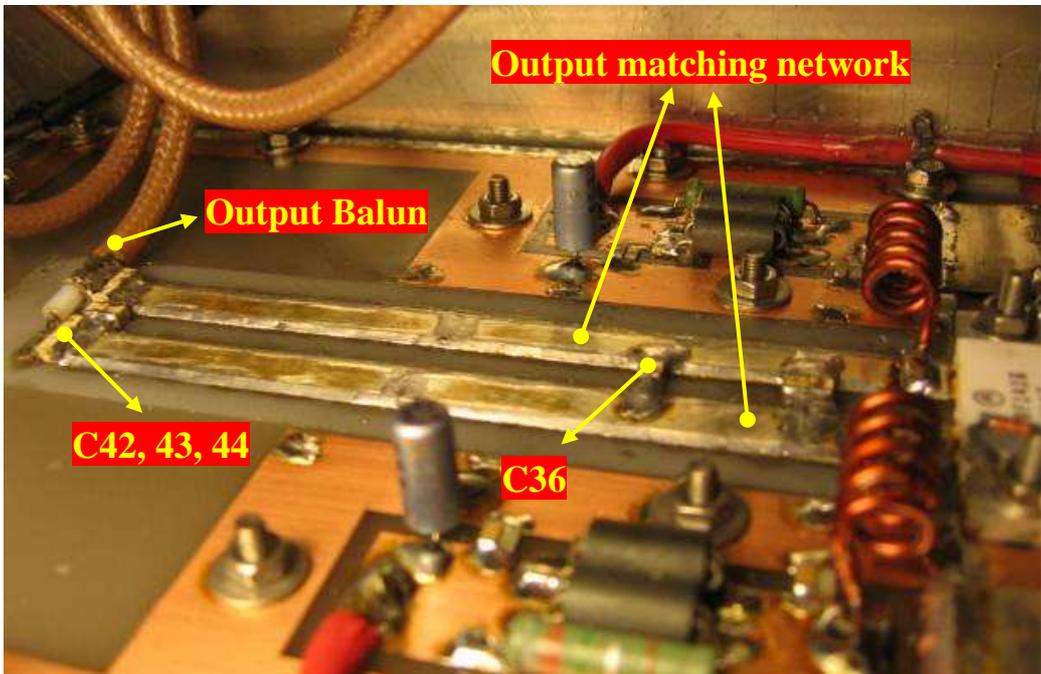
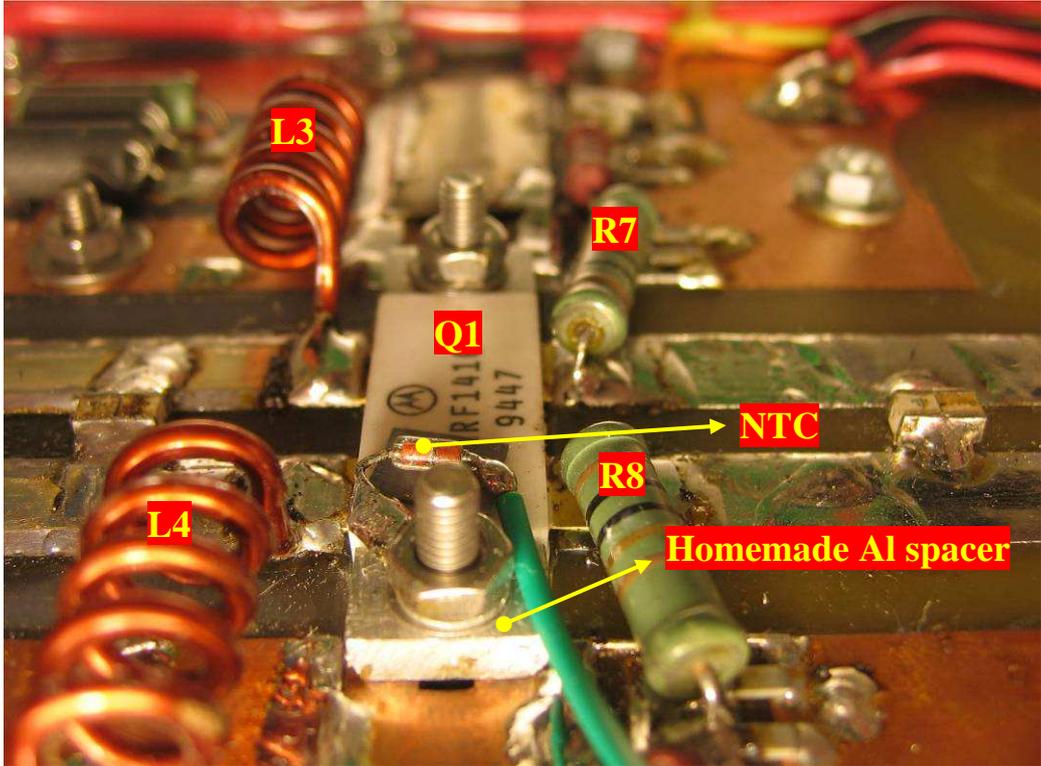
From a very subjective point of view, excessive splattering has never been reported, even by nearby stations.
The current drawn to achieve full output power lies around **20 A under 28 V**, yielding in an **efficiency of 53%**.

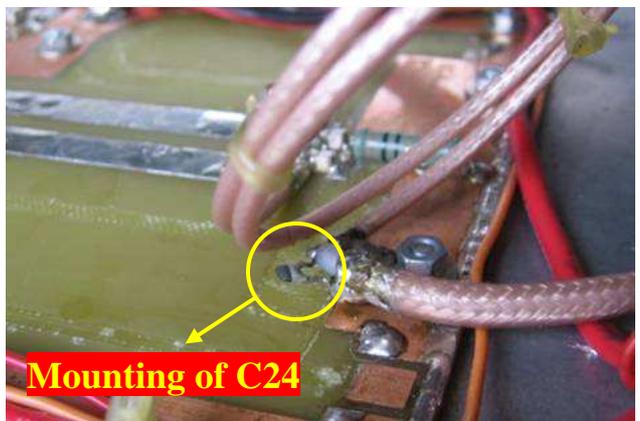
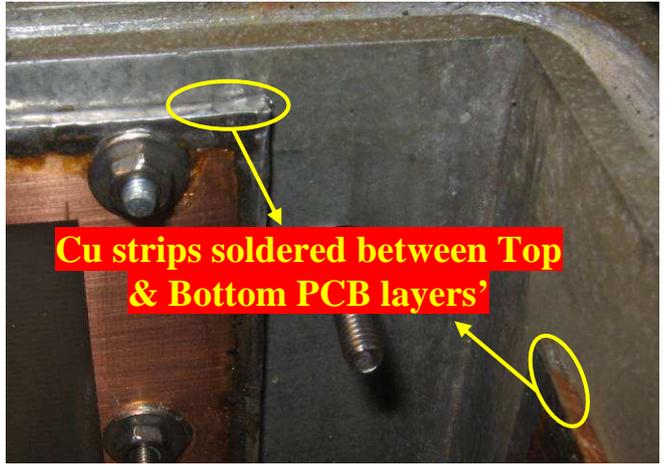
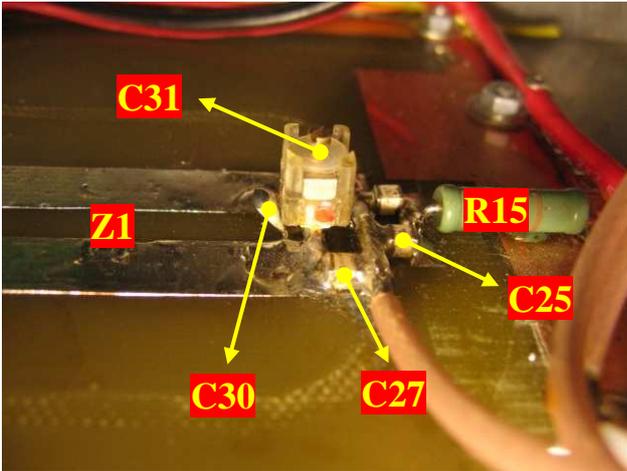
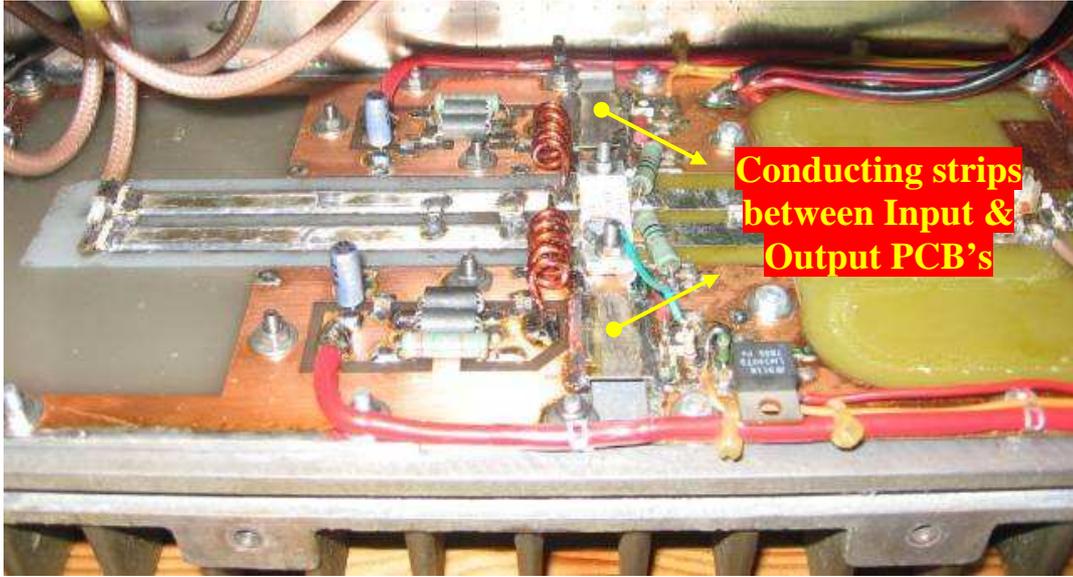
8. Pictures (zoom for close-up details)

This section shows in pictures the building details of the amplifier.









9. Appendix

Appendix 1 : Data sheet of the MRF141G

M/A-COM

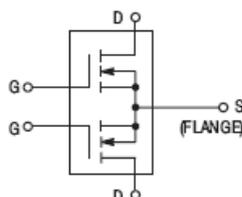
SEMICONDUCTOR TECHNICAL DATA

Order this document
by MRF141G/D

The RF MOSFET Line RF Power Field-Effect Transistor N-Channel Enhancement-Mode MOSFET

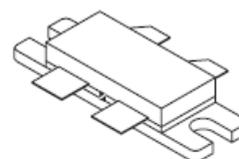
Designed for broadband commercial and military applications at frequencies to 175 MHz. The high power, high gain and broadband performance of this device makes possible solid state transmitters for FM broadcast or TV channel frequency bands.

- Guaranteed Performance at 175 MHz, 28 V:
Output Power — 300 W
Gain — 12 dB (14 dB Typ)
Efficiency — 50%
- Low Thermal Resistance — 0.35°C/W
- Ruggedness Tested at Rated Output Power
- Nitride Passivated Die for Enhanced Reliability



MRF141G

300 W, 28 V, 175 MHz
N-CHANNEL
BROADBAND
RF POWER MOSFET



CASE 375-04, STYLE 2

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	65	Vdc
Drain-Gate Voltage	V_{DGO}	65	Vdc
Gate-Source Voltage	V_{GS}	±40	Vdc
Drain Current — Continuous	I_D	32	Adc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	500 2.85	Watts W/°C
Storage Temperature Range	T_{stg}	-65 to +150	°C
Operating Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.35	°C/W

NOTE — **CAUTION** — MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Drain-Source Breakdown Voltage ($V_{GS} = 0, I_D = 100 \text{ mA}$)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current ($V_{DS} = 28 \text{ V}, V_{GS} = 0$)	I_{DSS}	—	—	5.0	mAdc
Gate-Body Leakage Current ($V_{GS} = 20 \text{ V}, V_{DS} = 0$)	I_{GSS}	—	—	1.0	μAdc

ON CHARACTERISTICS (1)					
Gate Threshold Voltage ($V_{DS} = 10 \text{ V}, I_D = 100 \text{ mA}$)	$V_{GS(th)}$	1.0	3.0	5.0	Vdc
Drain-Source On-Voltage ($V_{GS} = 10 \text{ V}, I_D = 10 \text{ A}$)	$V_{DS(on)}$	0.1	0.9	1.5	Vdc
Forward Transconductance ($V_{DS} = 10 \text{ V}, I_D = 5.0 \text{ A}$)	g_{fs}	5.0	7.0	—	mhos

DYNAMIC CHARACTERISTICS (1)					
Input Capacitance ($V_{DS} = 28 \text{ V}, V_{GS} = 0, f = 1.0 \text{ MHz}$)	C_{iss}	—	350	—	pF
Output Capacitance ($V_{DS} = 28 \text{ V}, V_{GS} = 0, f = 1.0 \text{ MHz}$)	C_{oss}	—	420	—	pF
Reverse Transfer Capacitance ($V_{DS} = 28 \text{ V}, V_{GS} = 0, f = 1.0 \text{ MHz}$)	C_{rss}	—	35	—	pF

FUNCTIONAL TESTS (2)					
Common Source Amplifier Power Gain ($V_{DD} = 28 \text{ V}, P_{out} = 300 \text{ W}, I_{DQ} = 500 \text{ mA}, f = 175 \text{ MHz}$)	G_{ps}	12	14	—	dB
Drain Efficiency ($V_{DD} = 28 \text{ V}, P_{out} = 300 \text{ W}, f = 175 \text{ MHz}, I_D (\text{Max}) = 21.4 \text{ A}$)	η	45	55	—	%
Load Mismatch ($V_{DD} = 28 \text{ V}, P_{out} = 300 \text{ W}, I_{DQ} = 500 \text{ mA}, f = 175 \text{ MHz}, \text{VSWR } 5:1 \text{ at all Phase Angles}$)	ψ	No Degradation in Output Power			

NOTES:

- Each side measured separately.
- Measured in push-pull configuration.

TYPICAL CHARACTERISTICS

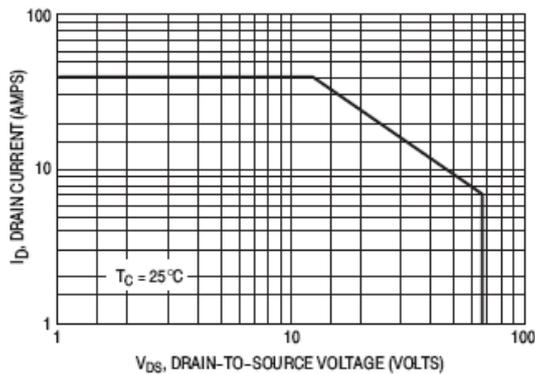


Figure 2. DC Safe Operating Area

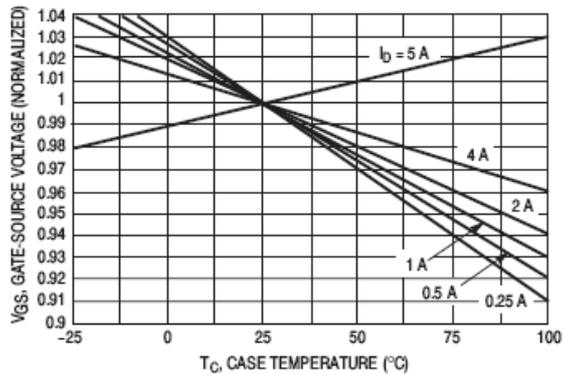
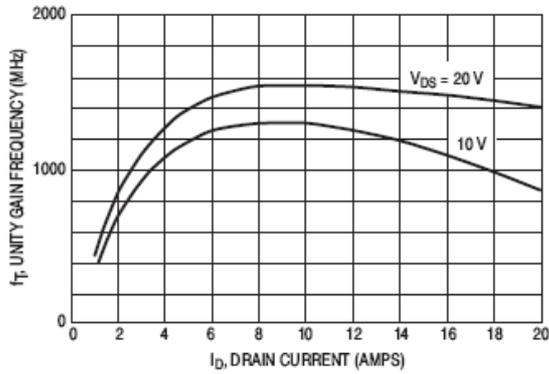


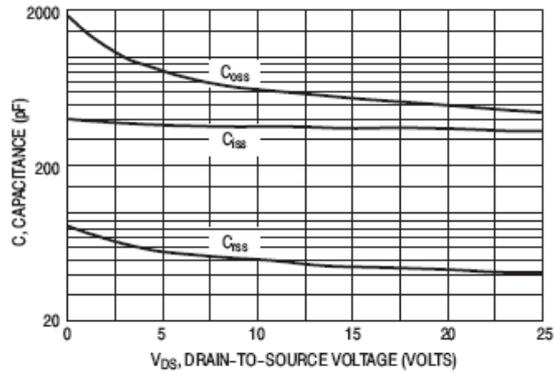
Figure 3. Gate-Source Voltage versus Case Temperature

TYPICAL CHARACTERISTICS



NOTE: Data shown applies to each half of MRF141G.

Figure 4. Common Source Unity Gain Frequency versus Drain Current



NOTE: Data shown applies to each half of MRF141G.

Figure 5. Capacitance versus Drain-Source Voltage

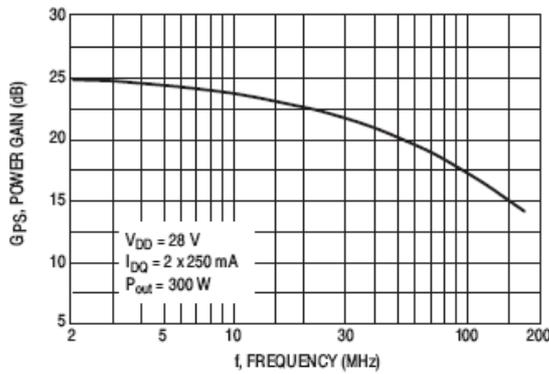


Figure 6. Power Gain versus Frequency

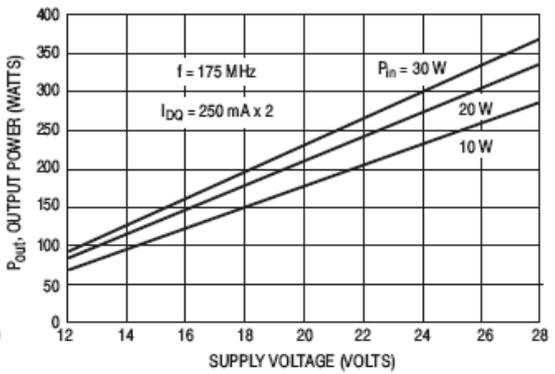
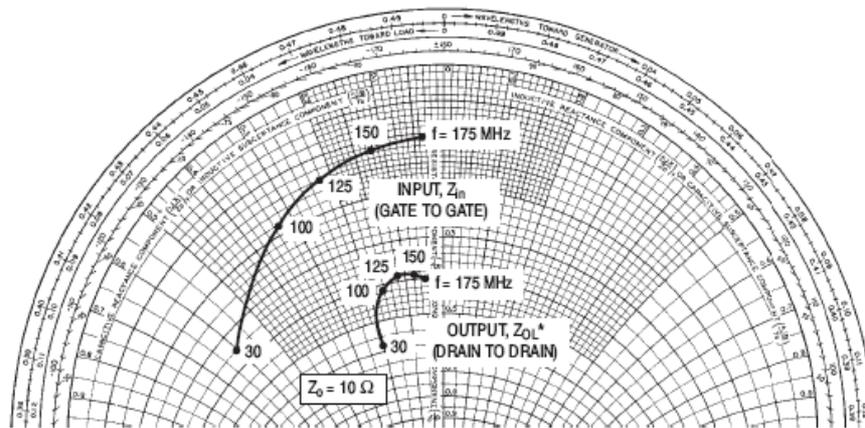


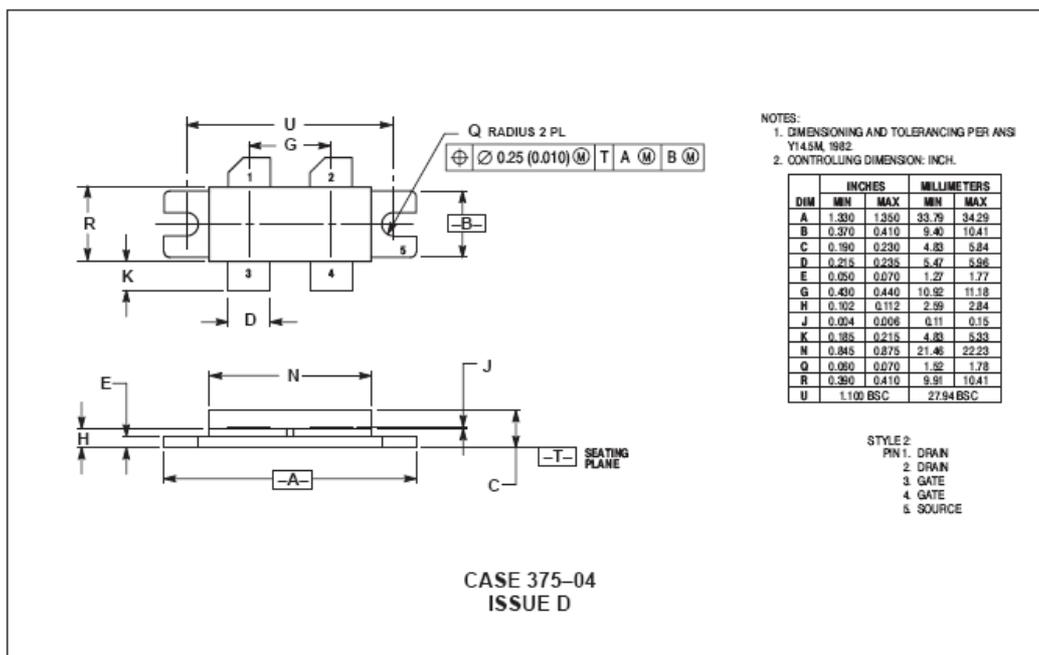
Figure 7. Output Power versus Supply Voltage



Z_{OL}^* = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage and frequency.

Figure 8. Input and Output Impedances

PACKAGE DIMENSIONS



Appendix 2 : Data sheet of the C31 (RF board) Philips variable capacitor

FILM DIELECTRIC TRIMMERS

Philips type 222 809

- High temperature type
- Housing dimensions 8 mm x 8 mm x 9 mm
- For basic grid of 2.54 mm
- For professional applications, e.g. fine adjustment of h.f. tuned circuits

QUICK REFERENCE DATA

C_{\min}/C_{\max}	0.5/2 to 2/18 pF
Rated voltage (DC)	300 V
Housing diameter	8 mm x 8 mm x 9 mm
Climatic category (IEC 88)	40/125/21
Related specification	IEC 418-1 and 4

Selection chart

Vertical spindle, top and bottom adjustment.

value (pF) C_{\min}/C_{\max}	round head	hex. head
	catalogue number	catalogue number
0.5/2	2222 809 05011	2222 809 05021
1.2/3.5	2222 809 05215	2222 809 05225
1.8/10	2222 809 05216	2222 809 05226
2/18	2222 809 05217	2222 809 05227

DESCRIPTION

The trimmers consist of a polysulphone housing, brass rotor and plated brass stator with a PTFE film as the dielectric. The stator plates with their tag are heat sealed to the housing. The rotor contact surfaces are plated to ensure a long life and a stable contact even under severe climatic conditions. Flux absorption between the vanes is prevented. A colour dot indicates the maximum capacitance. The trimmers have top and bottom adjustment. Top adjustment should be done by means of a screw driver and bottom adjustment by means of the key as shown in Fig.4.

MECHANICAL DATA

Outlines	see Fig.1
Effective angle of rotation	180°
Operating torque	1 to 15 mNm
$C_{max} = 3,5 \text{ pF}$	2.5 to 20 mNm
$C_{max} = 10 \text{ and } 18 \text{ pF}$	
Maximum axial thrust ($\Delta C \leq 0,3\%$ of C_{max})	2 N
Mass	approx. 0.45 g

Mounting

The trimmers can be mounted on printed-circuit boards with hole diameter min. 2,54 mm. For hole pattern, see Fig.3.

Soldering conditions: max. 260 °C, max. 10 s. (See Tests and Requirements).

ELECTRICAL DATA

Rated voltage (DC)	300 V
Test voltage (DC) for 1 min.	600 V
Contact resistance	max. 5 mΩ
Insulation resistance between stator and rotor	min. 10 000 MΩ
Category temperature range	-40 to +125 °C
Climatic category (IEC 68)	40/125/21
Minimum storage temperature	-55 °C

Table 1

guaranteed max. C_{min} min. C_{max} at 200 kHz pF	catalogue number	shape of head	$\tan \delta$ at $C_{max} \times 10^{-4}$		temp. coeff. (note 1) $10^{-9}/K$	min. f_{res} at C_{max} MHz	colour of base	smallest packing quantity
			1 MHz	100 MHz				
0.5/2	2222 809 05011	round hex	≤ 10	≤ 20	-250 ± 200	1200	no	140
	2222 809 05021							
1.2/3.5	2222 809 05215	round hex	≤ 10	≤ 20	-250 ± 150	850	orange	140
	2222 809 05225							
1.8/10	2222 809 05216	round hex	≤ 10	≤ 20	-350 ± 150	580	white	140
	2222 809 05226							
2/18	2222 809 05217	round hex	≤ 10	≤ 25	-350 ± 150	360	red	140
	2222 809 05227							

Note

1. C at 60% to 80% of C_{max} ; T from +20 °C to +125 °C.

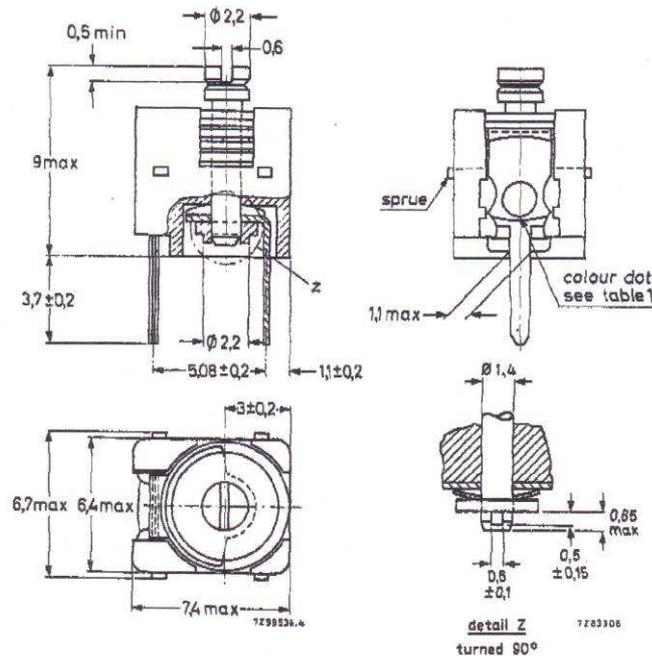
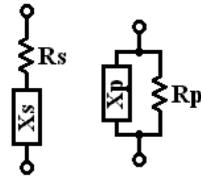


Fig.1 Trimmers 2222 809 05... series, round head.

Appendix 3 : Series \leftrightarrow parallel impedance transformation equations



$$R_p = \frac{R_s^2 + X_s^2}{R_s} \quad X_p = \frac{R_s^2 + X_s^2}{X_s}$$

$$R_s = \frac{R_p \cdot X_p^2}{R_p^2 + X_p^2} \quad X_s = \frac{R_p^2 \cdot X_p}{R_p^2 + X_p^2}$$

10. References

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- [2] : “RF Power Device Impedances : Practical Considerations”, Motorola AN1526, 1991
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- [4] : “BLF278” data sheet, Philips, October 1996
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